Data Sheet: Technical Data

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CCFC3007PT Microcontroller Data Sheet

- Three main CPUs, single issue, 32-bit CPU core complexes (C3007), one of which is a dedicated lockstep core.
  - Power Architecture® embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - 16 KB Local instruction RAM and 64 KB local data RAM
  - 16 KB I-Cache and 4 KB D-Cache
- I/O Processor, dual issue, 32-bit CPU core complex (C2004), with
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - Lightweight Signal Processing Auxiliary Processing Unit (LSP APU) instruction support for digital signal processing (DSP)
  - 16 KB Local instruction RAM and 64 KB local data RAM
  - 8 KB I-Cache
- 13568 KB on-chip flash
  - Include 13056Kbytes Code flash supports read during program and erase operations, and 512KBytes allowing EEPROM emulation
- 1.5 MB System RAM
- Multichannel direct memory access controllers (eDMA): 2 x 64 channels per eDMA (128 channels total)
- Triple Interrupt controller (INTC)
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Dual crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters with end-to-end ECC
- Real Time Clock / Autonomous Periodic Interrupt (RTC/API)
- Hardware Security Module (HSM) to provide robust integrity checking of flash memory
- System Integration Unit Lite (SIUL)
- Boot Assist Module (BAM) supports factory programming using serial bootload through LINFlexD_0 or MCAN1
- GTM104 — generic timer module
- Enhanced analog-to-digital converter system with
  - Ten separate 12-bit Enhanced Queued analog converters
  - Eight separate 16-bit Sigma-Delta analog converters
- Eight deserial serial peripheral interface (DSPI) modules
- Two Peripheral Sensor Interface (PSI5) controllers support 5 channels
- Two I2C controllers support master and slave
- Two SENT Receivers support 15 channels
- Two CSENT with 15 channels which support sent frame receiver and transmit
- Two eMIOS controller support 32 channels
- Three eTPU co-processor support 96 channels
- Sixteen LINFlexD support LIN Master/Slave and UART communication interface
- Twelve modular controller area network (MCAN) modules and three time-triggered controller area networks (M-TTCAN)
- Two CAST CANFD Controller which support controller area network and time-triggered controller area networks
- One DWC_ether_qos Ethernet Controller (MAC) and TSN feature :
  - supports 10 and 100 Mbps Ethernet/IEEE 802.3 networks
  - IEEE 802.1Qbv-2015, Enhancements to Scheduling Traffic
  - IEEE802.1Qbu/802.3br, Frame preemption and Interspersing Express Traffic
- Two I2S(SAI)
- Two QSPI which support 4 bit width transmit
- Nexus deve10pment interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG)(IEEE 1149.1)
- Self-test capability

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1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the CCFC3007PT series of microcontroller units (MCUs). For functional characteristics, see the *CCFC3007PT Microcontroller Reference Manual*.

1.2 Description

This family of MCUs is targeted at automotive powertrain controller and chassis control applications from single cylinder motorcycles at the very bottom end; through 4 to 8 cylinder gasoline and diesel engines; transmission control; steering and breaking applications; to high end hybrid and advanced combustion systems at the top end.

Many of the applications are considered to be functionally safe and the family is designed to achieve ISO26262 ASIL-D compliance.

Version	CCFC3007BCT64L9	CCFC3007BCT192L9	CCFC3007BCT192B4	CCFC3007PTT192B2	CCFC3007PTT192B4	CCFC3007PTT192B6
Type	32 bit multiprocessor	32 bit multiprocessor	32 bit multiprocessor	32 bit multiprocessor	32 bit multiprocessor	32 bit multiprocessor
CPU	2*C3007+C3007 (lockstep)	2*C3007+C3007 (lockstep)	2*C3007+C3007 (lockstep)	2*C3007+C3007 (lockstep)	2*C3007+C3007 (lockstep)	2*C3007+C3007 (lockstep)
Frequence	300MHZ	300MHZ	300MHZ	300MHZ	300MHZ	300MHZ
RAM	640K	640K	640K	1.5M	1.5M	1.5M
C-flash	4M	12M	12M	12M	12M	12M
D-flash	512K	512K	512K	512K	512K	512K
Package	LQFP216	LQFP216	BGA416	BGA292	BGA416	BGA516
Operating temperature (℃)	-40°C ~ 125°C (TA)	-40°C ~ 125°C (TA)	-40°C ~ 125°C (TA)	-40°C ~ 125°C (TA)	-40°C ~ 125°C (TA)	-40°C ~ 125°C (TA)
Operating voltage (V)	3.3/5	3.3/5	3.3/5	3.3/5	3.3/5	3.3/5
I/O number	153	153	333	187	333	378
CAN(FD) (ch)	10（CanFD)	10（CanFD)	12（CanFD)	12（CanFD)	12（CanFD)	14（CanFD)
LIN (ch)	11	11	16	16	16	16
SPI (ch)	6	6	8	8	8	8
QSPI (ch)	2	2	2	2	2	2
I2C (ch)	2	2	2	2	2	2
ETHER	1	1	1	1	1	1
SENT	13	13	15	15	15	15
PSI5	3	3	5	4	5	5
AD (ch)	36	36	70	45	70	84
DMA	128	128	128	128	128	128
eTPU	-	-	-	96	96	96
GTM	Y	Y	Y	Y	Y	Y
eMIOS (ch)	64	64	64	64	64	64
HSM	Y	Y	Y	Y	Y	Y
Reliability Functional Safety	AEC-Q100 ASIL-B	AEC-Q100 ASIL-B	AEC-Q100 ASIL-B	AEC-Q100 ASIL-D	AEC-Q100 ASIL-D	AEC-Q100 ASIL-D
Replaceability	MPC5775E/TC367	MPC5775E/TC367	MPC5775E/TC367	MPC5777M/TC387	MPC5777M/TC387	MPC5777M/TC387
Mass production time	2023Q2	2023Q2	2023Q2	2023Q3	2023Q3	2023Q3

1.3 Device feature

Table 1. CCFC3007PT feature

Feature		CCFC3007PT
Process		TSMC 40 nm
Safety Goal		ASIL-D
Main processor	Core	C3007
	Number of main cores	2
	Number of checker cores	1
	Local RAM (per main core)	16 KB Instruction 64 KB Data
	Single precision floating point	Yes
	LSP	No
	VLE	Yes
	Cache	16 KB Instruction 4 KB Data
I/O processor	Core	C2004
	Local RAM	16 KB instruction 64 KB Data
	Single precision floating point	Yes
	LSP	Yes
	VLE	Yes
	Cache	8 KB instruction
HSM processor	Core	C2002
	Security Grade	Evita-Full
	Symmetric-algorithm	AES/DES3/SM1/SM4
	Asymmetric-algorithm	SM2/RSA-4096/ECC
	Hash-algorithm	SHA/SHA3/SM3/MD5/RIPEMD160
Main processor frequency		300 MHz[1]
I/O processor frequency		200 MHz
HSM processor frequency		100 MHz
MMU entries		0
MPU		Yes
Semaphores		Yes

Table 1. CCFC3007PT feature (continued)

Feature	CCFC3007PT
CRC channels	2
Software watchdog timer (Task SWT/Safety SWT)	4 (2/2)
Core Nexus class	3+
Debug and calibration interface (DCI) / run control module	Yes
System SRAM	1.5MB
Flash memory	13056KB
Flash memory fetch accelerator	4 × 256 bit
Data flash memory (EEPROM)	512 KB
Flash memory overlay RAM	16 KB
DMA channels	2 × 64
DMA Nexus Class	3+
RTC/API	1
LINFlexD	16
MCAN/TTCAN	12/3
CANFD	2
QSPI(4 bit width)	2
DSPI	8
Microsecond bus downlink	Yes
SENT bus	15
CSENT bus	15
I^2C	2
I^2S(SAI)	2
PSI5 bus	5
PSI5-S UART-to-PSI5 interface	Yes
FlexRay	2 × dual channel
DWC_ether_qos	MII / RMII/TSN
System timers	8 PIT channels 3 AUTOSAR® (STM) 64-bit PIT
BOSCH® GTM Timer[2]	Yes
GTM RAM	58 KB
Interrupt controller	926 sources
ADC (EQADC)	5 × 2

Table 1. CCFC3007PT feature (continued)

Feature	CCFC3007PT
eTPU channels	96
eMIOS channels	2 × 16
ADC (SD)	8
Temperature sensor	Yes
Self test controller	Yes
PLL	Dual PLL with FM
Integrated linear voltage regulator	None
External power supplies	5 V 3.3 V[3] 1.1 V
Low-power modes	Stop mode Slow mode Standby mode
Packages	HQFP216/416 PBGA[4]

1 Includes four user-programmable CPU cores and one safety core. The main computational shell consists of dual C3007 CPUs operating at 300 MHz with a third identical core running as a safety checker core in delayed lockstep mode with one of the dual C3007 cores. The I/O subsystem includes a CPU targeted at managing the peripherals. This is an C2004 CPU running at 200 MHz. The fifth CPU is an C2002 running at 100 MHz and is embedded in the Hardware Security Module. All CPUs are compatible with the Power Architecture.

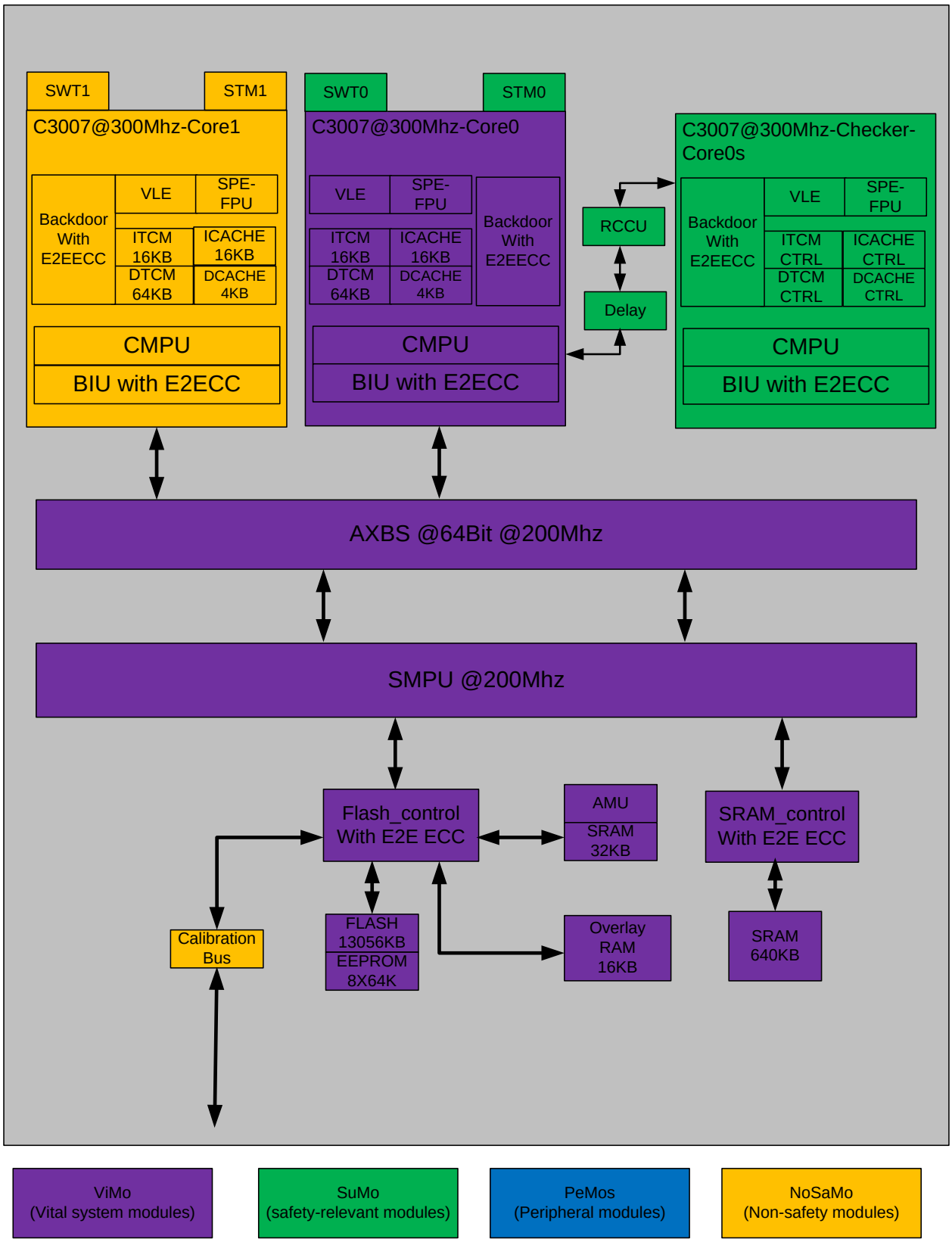
2 BOSCH® is a registered trademark of Robert Bosch GmbH.

3 3.3V supply is for Ethernet phy interface

4 TBD

1.4 Block diagram

The figures below show the top-level block diagrams.



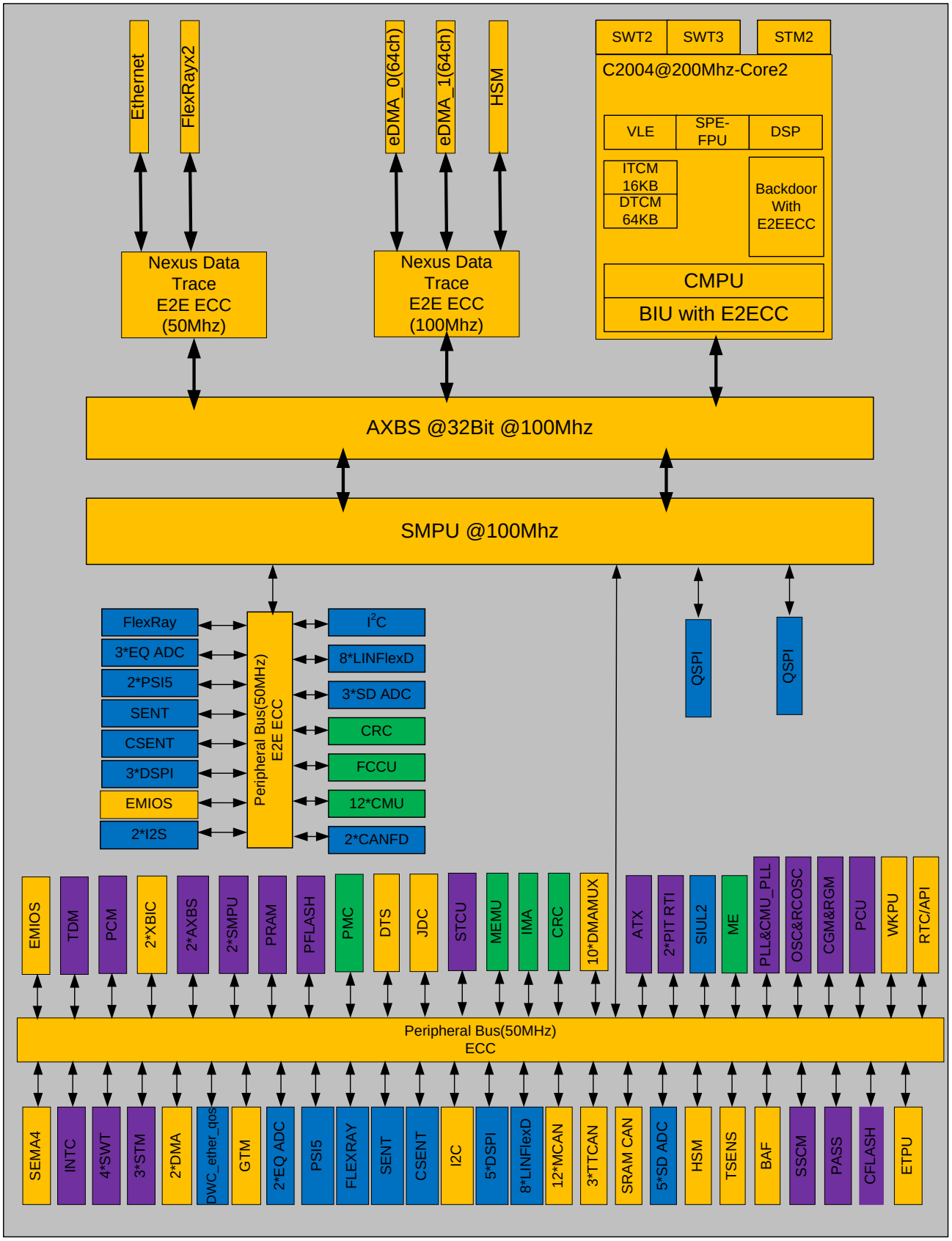


Figure 1. Block diagram

2 Package pinouts and signal descriptions

2.1 Package pinouts

The available BGA / HQFP pinouts and the ballmap are provided in CCFC3007PT pinmux and pinout.xlsx

The BGA ballmap package pinouts for the 416 production and emulation devices are shown in the table CCFC3007PTT192B4

2.2 Functional port pins

Please see the table CCFC3007PT_pinmux in CCFC3007PT pinmux and pinout.xlsx

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

NOTE

Within this document, $V_{DD\_HV\_IO}$ refers to supply pins $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_FLEX}$ and $V_{DD\_HV\_IO\_5V}$. $V_{DD\_HV\_ADV}$ refers to ADC supply pins $V_{DD\_HV\_ADV\_S}$ and $V_{DD\_HV\_ADV\_D}$. $V_{DD\_HV\_ADR}$ refers to ADC reference pins $V_{DD\_HV\_ADR\_S}$ and $V_{DD\_HV\_ADR\_D}$. $V_{SS\_HV\_ADV}$ refers to ADC ground pins $V_{SS\_HV\_ADV\_S}$ and $V_{SS\_HV\_ADV\_D}$. $V_{SS\_HV\_ADR}$ refers to ADC reference pins $V_{SS\_HV\_ADR\_S}$ and $V_{SS\_HV\_ADR\_D}$.

3.2 Absolute maximum ratings

Table 6 describes the maximum ratings of the device.

Table 2. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{DD_LV}	SR	1.1 V core supply voltage	—	–0.3	TBD	V
$V_{DD\_HV\_IO}$	SR	I/O supply voltage[2]	—	–0.3	6.0	V
$V_{DD\_HV\_PMC}$	SR	Power Management Controller supply voltage	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$	SR	Flash core voltage	—	–0.3	3.6	V
$V_{SS\_HV\_ADV}$[3]	SR	SAR and S/D ADC ground voltage	Reference to V	–0.3	0.3	V
$V_{DD\_HV\_ADV}$[4]	SR	SAR and S/D ADC supply voltage	Reference to corresponding $V_{SS\_HV\_ADV}$	–0.3	6.0	V
$V_{SS\_HV\_ADR}$[5]	SR	SAR and S/D ADC low reference	Reference to V_{SS_LV}	–0.3	0.3	V
$V_{DD\_HV\_ADR}$[6]	SR	SAR and S/D ADC high reference	Reference to corresponding $V_{SS\_HV\_ADR}$	–0.3	6.0	V
V_{IN}	SR	I/O input voltage range[7]	—	–0.3	6.0	V
			Relative to V_{SS_LV}[8]	–0.3	—	
			Relative to $V_{DD\_HV\_IO}$[8]	—	0.3	
I_{INJD}	SR	Maximum DC injection current for digital pad	Per pin, applies to all digital pins	–5	5	mA
I_{INJA}	SR	Maximum DC injection current for analog pad	Per pin, applies to all analog pins	–5	5	mA
I_{MAXD}	SR	Maximum output DC current when driven	Medium	–3.8	3.8	mA
			Fast	–20	20	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 $V_{DD\_HV\_IO}$ applies to $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_FLEX}$ and $V_{DD\_HV\_IO\_5V}$ I/O power supplies.

[3] Includes ADC grounds $V_{SS\_HV\_ADV\_S}$ and $V_{SS\_HV\_ADV\_D}$.

[4] Includes ADC supplies $V_{DD\_HV\_ADV\_S}$ and $V_{DD\_HV\_ADV\_D}$.

[5] Includes ADC low references $V_{SS\_HV\_ADR\_S}$ and $V_{SS\_HV\_ADR\_D}$.

[6] Includes ADC high references $V_{DD\_HV\_ADR\_S}$ and $V_{DD\_HV\_ADR\_D}$.

[7] The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies significantly across process and temperature, but a value of 0.3V can be used for nominal calculations.

[8] $V_{DD\_HV\_IO}/V_{SS\_HV\_IO}$ refers to supply pins and corresponding grounds: $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_IO\_5V}$, $V_{DD\_HV\_OSC}$, $V_{DD\_HV\_PMC}$.

3.3 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

Table 3. ESD ratings[1,2]

Parameter	Conditions	Value	Unit
ESD for Human Body Model (HBM)[3]	All pins	2000	V
ESD for field induced Charged Device Model (CDM)[4]	All pins	500	V
	Corner pins	750	

[1] All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

[2] Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification”

[3] This parameter tested in conformity with ANSI/ESDA/JEDEC JS-001 Electrostatic Discharge Sensitivity Testing

[4] This parameter tested in conformity with ANSI/ESD S5.3.1-2009 Charged Device Model - Component Level

3.4 Operating conditions

The following table describes the operating conditions for the device for which all specifications in the data sheet are valid, except where explicitly noted.

The device operating conditions must not be exceeded or the functionality of the device is not guaranteed.

Table 4. Device operating conditions[1]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Frequency							
f_{SYS}	SR	Device operating frequency[2]	T_J = –40 °C to 150 °C	—	—	300	MHz

Table 4. Device operating conditions[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Temperature							
T_J	SR	Operating temperature range - junction	—	–40.0	—	150.0	°C
T_A (T_L to T_H)	SR	Ambient operating temperature range	—	–40.0	—	125.0	°C
Voltage							
V_{DD_LV}	SR	External core supply voltage[3,4]	—	0.99	—	1.21	V
$V_{DD\_HV\_IO\_MAIN}$	SR	I/O supply voltage	—	3.0	—	5.5[12]	V
$V_{DD\_HV\_IO\_5v}$	SR	Ethernet I/O predriver supply voltage	—	4.5	—	5.5	V
$V_{DD\_HV\_IO\_FLEX}$	SR	Ethernet I/O supply voltage	5 V range	3.0	—	5.5	V
			3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_OSC}$	SR	Oscillator supply voltage		3.0	—	5.5	V
$V_{DD\_HV\_PMC}$	SR	Power Management Controller (PMC) supply voltage	Full functionality	3.0[5]	—	5.5	V
$V_{DD\_HV\_ADV}$	SR	SARADC, SDADC Power supply voltage	—	3.0	—	5.5	V
$V_{DD\_HV\_ADR\_D}$	SR	SD ADC supply reference voltage	Full SNR	3.0		5.5	V
$V_{DD\_HV\_ADR\_D}$ – $V_{DD\_HV\_ADV\_D}$	SR	SD ADC reference differential voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR\_D}$	SR	SD ADC ground reference voltage	—	$V_{SS\_HV\_ADV\_D}$			V
$V_{SS\_HV\_ADR\_D}$ – $V_{SS\_HV\_ADV\_D}$	SR	$V_{SS\_HV\_ADR\_D}$ differential voltage	—	–25	—	25	mV
$V_{DD\_HV\_ADR\_S}$	SR	SARADC reference	—	3.0	$V_{DD\_HV\_ADV\_S}$	5.5	V
$V_{SS\_HV\_ADR\_S}$	SR	SAR ADC ground reference voltage	—	$V_{SS\_HV\_ADV\_S}$			V
$V_{DD\_HV\_ADR\_S}$ – $V_{DD\_HV\_ADV\_S}$	SR	SARADC reference differential voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR\_S}$ – $V_{SS\_HV\_ADV\_S}$	SR	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–25	—	25	mV
$V_{SS\_HV\_ADV}$ – V_{SS_LV}	SR	$V_{SS\_HV\_ADV}$ differential voltage	—	–25	—	25	mV
V_{RAMP_LV}	SR	Slew rate on core power supply pins	—	—	—	100	V/ms
V_{RAMP_HV}	SR	Slew rate on HV power supply pins	—	—	—	100	V/ms
V_{por_rel}	CC	POR release trip point	-40 °C < Tj < 150 °C	—	2.84	—	V
V_{IN}	SR	I/O input voltage range	—	0	—	5.5	V

1 The ranges in this table are design targets and actual data may vary in the given range.

2 Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the *CCFC3007PT Microcontroller Reference Manual* for more information on the clock limitations for the various IP blocks on the device.

3 Core voltage as measured on device pin to guarantee published silicon performance.

4 During power ramp, voltage measured on silicon might be lower. maximum performance is not guaranteed, but correct silicon operation is guaranteed. Refer to the Power Management and Reset Generation Module chapters in the *CCFC3007PT Microcontroller Reference Manual* for further information.

5 During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN}$ physical I/O segment.

3.5 I/O pad electrical characteristics

3.5.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Medium pads—provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—provide maximum speed. These are used for Ethernet communication interface IO.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

3.5.2 I/O input DC characteristics

Table 5 provides input DC electrical characteristics as described in Figure 2.

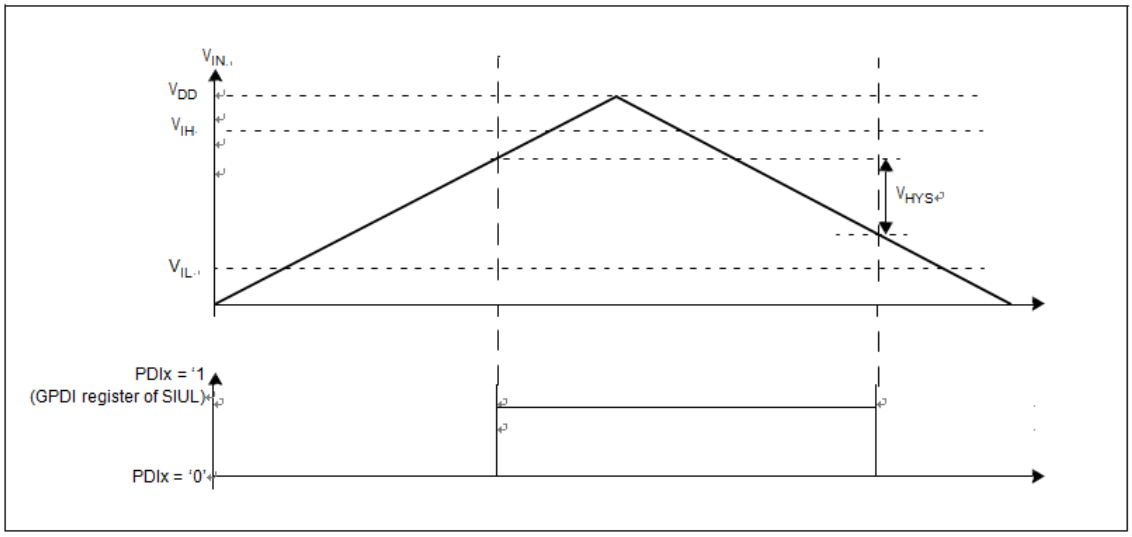


Figure 2. I/O input DC electrical characteristics definition

Table 5. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		−0.4	—	$0.35V_{DD}$	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	
I_{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T_A = −40 °C	—	2	200	nA
		D			T_A = 25 °C	—	2	200	
		D			T_A = 85 °C	—	5	300	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	

1 V_{DD} stands for $V_{DD\_HV\_IO\_MAIN}$,V_{DD} = 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

3.5.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 6 provides weak pull characteristics for I/O pads when in MEDIUM configuration
- Table 7 provides weak pull characteristics for I/O pads when in FAST configuration
- Table 8 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 9 provides output driver characteristics for I/O pads when in FAST configuration.

Table 6. Medium I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	V_{IN} = V_{IL}, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[2]	10	—	250	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	V_{IN} = V_{IH}, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	

1 V_{DD} stands for $V_{DD\_HV\_IO\_MAIN}$,T_A = −40 to 125 °C, unless otherwise specified.

Table 7. FAST I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$	$V_{DD\_HV\_IO\_FLEX}$ = 5.0 V ± 10%	79	—	119	µA
		C			$V_{DD\_HV\_IO\_FLEX}$ = 3.3 V ± 10%	30	—	66	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$	$V_{DD\_HV\_IO\_FLEX}$ = 5.0 V ± 10%	82	—	119	µA
		C			$V_{DD\_HV\_IO\_FLEX}$ = 3.3 V ± 10%	31	—	72	

[1] T_A = −40 to 125 °C, unless otherwise specified.

Table 8. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = −3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = −2 mA,V_{DD} = 5.0 V ± 10%, PAD3V5V = 0(recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = −1 mA,V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = −100 µA,V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3.8 mA,V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		P			I_{OL} = 2 mA,V_{DD} = 5.0 V ± 10%, PAD3V5V = 0(recommended)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA,V_{DD} = 5.0 V ± 10%, PAD3V5V = 1	—	—	$0.1V_{DD}$	
		C			I_{OL} = 100 µA,V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	

[1] V_{DD} stands for $V_{DD\_HV\_IO\_MAIN}$, T_A = −40 to 125 °C, unless otherwise specified

Table 9. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull	I_{OH} = −20 mA	0.8 $V_{DD\_HV\_IO\_FLEX}$	—	—	V
V_{OL}	CC	P	Output low level FAST configuration	Push Pull	I_{OL} = 20 mA	—	—	0.2 $V_{DD\_HV\_IO\_FLEX}$	V

[1] $V_{DD\_HV\_IO\_FLEX}$ = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

3.6 Reset pad ($\overline{\text{PORST}}$, $\overline{\text{ESR0}}$) electrical characteristics

The device implements a dedicated bidirectional reset pin ($\overline{\text{PORST}}$).

NOTE

$\overline{\text{PORST}}$ pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 kΩ.

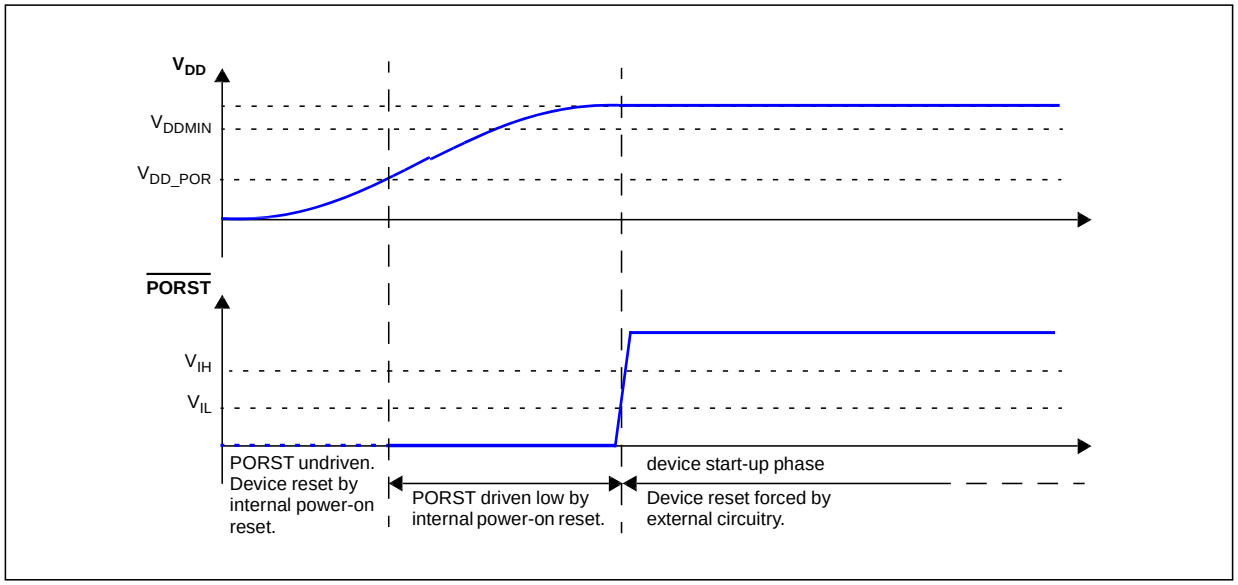


Figure 3. Start-up reset requirements

Figure 4 describes device behavior depending on supply signal on $\overline{\text{PORST}}$:

1. $\overline{\text{PORST}}$ low pulse amplitude is too low—it is filtered by input buffer hysteresis. Device remains in current state.
2. $\overline{\text{PORST}}$ low pulse duration is too short—it is filtered by a low pass filter. Device remains in current state.
3. $\overline{\text{PORST}}$ low pulse generates a reset:
   a) $\overline{\text{PORST}}$ low but initially filtered during at least W_{FRST}. Device remains initially in current state.
   b) $\overline{\text{PORST}}$ potentially filtered until W_{NFRST}. Device state is unknown: it may either be reset or remains in current state depending on other factors (temperature, voltage, device).
   c) $\overline{\text{PORST}}$ asserted for longer than W_{NFRST}. Device is under reset.

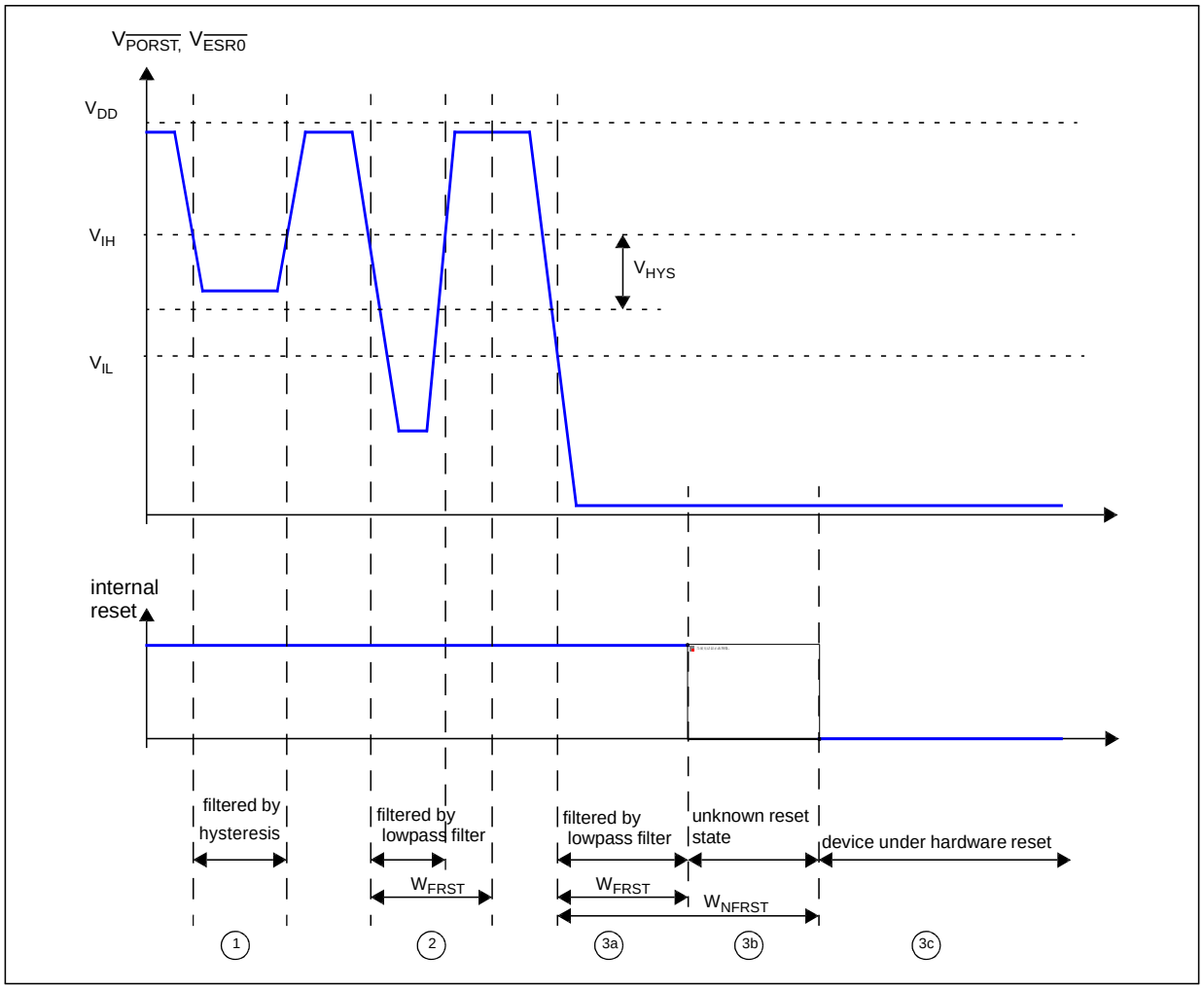


Figure 4. Noise filtering on reset signal

Table 10. Reset electrical characteristics

Symbol		Parameter	Conditions	Value[1]			Unit
				Min	Typ	Max	
V_{IH}	SR	Input high level TTL (Schmitt trigger)	—	2.2	—	$V_{DD\_HV\_IO}$ +0.4	V
V_{IL}	SR	Input low level TTL (Schmitt trigger)	—	–0.4	—	0.8	V
V_{HYS}	CC	Input hysteresis TTL (Schmitt trigger)	—	300	—	—	mV
V_{DD_POR}	CC	Minimum supply for strong pull-down activation	—	—	—	1.2	V

Table 10. Reset electrical characteristics (continued)

Symbol		Parameter	Conditions	Value[1]			Unit
				Min	Typ	Max	
I_{OL_R}	CC	Strong pull-down current[2]	Device under power-on reset $V_{DD\_HV\_IO} = V_{DD\_POR}$, $V_{OL} = 0.35 * V_{DD\_HV\_IO}$	0.2	—	—	mA
			Device under power-on reset 3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V, V_{OL} > 0.9 V	11	—	—	mA
$\|I_{WPU}\|$	CC	Weak pull-up current absolute value	ESR0 pin $V_{IN} = 0.69 * V_{DD\_HV\_IO}$	23	—	—	µA
			ESR0 pin $V_{IN} = 0.49 * V_{DD\_HV\_IO}$	—	—	82	
$\|I_{WPD}\|$	CC	Weak pull-down current absolute value	PORST pin $V_{IN} = 0.69 * V_{DD\_HV\_IO}$	—	—	130	µA
			PORST pin $V_{IN} = 0.49 * V_{DD\_HV\_IO}$	40	—	—	
W_{FRST}	SR	PORST and ESR0 input filtered pulse	—	—	—	500	ns
W_{NFRST}	SR	PORST and ESR0 input not filtered pulse	—	2000	—	—	ns
W_{FNMI}	SR	ESR1 input filtered pulse	—	—	—	40	ns
W_{NFNMI}	SR	ESR1 input not filtered pulse	—	1000	—	—	ns

1 An external 4.7 KOhm pull-up resistor is recommended to be used with the PORST and ESR0 pins for fast negation of the signals.

2 I_{OL_R} applies to both PORST and ESR0: Strong pull-down is active on PHASE0 for PORST. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for ESR0.

NOTE

$\overline{\text{PORST}}$ can optionally be connected to an external power-on supply circuitry.

NOTE

No restrictions exist on reset signal slew rate apart from absolute maximum rating compliance.

3.7 Oscillator and FMPLL

The Reference PLL (PLL0) and the System PLL (PLL1) generate the system and auxiliary clocks from the main oscillator driver.

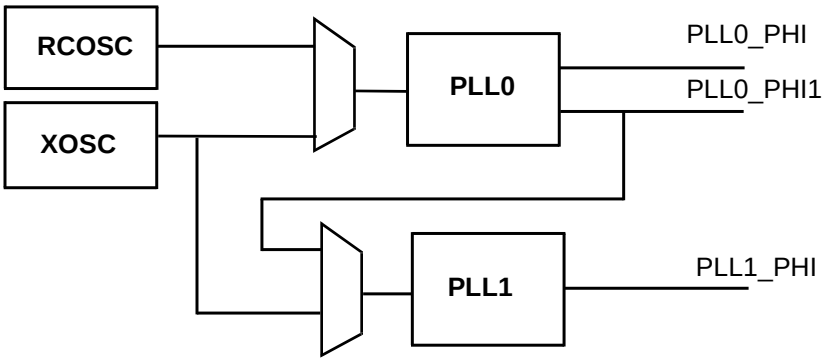


Figure 5. PLL integration

Table 11. PLL0 electrical characteristics[1]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{PLL0IN}	SR	PLL0 input clock	—	8	—	44	MHz
$f_{PLL0VCO}$	CC	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI}$	CC	PLL0 output frequency	—	4.762	—	400	MHz
$t_{PLL0LOCK}$	CC	PLL0 lock time	—	—	—	110	µs
$\lvert\Delta_{PLL0PHISPJ}\rvert$	CC	PLL0 period jitter	f_{VCO}= 800 MHz	—	50	200	ps
D_{TC}	CC	Output duty cycle		45	50	55	%

1 $V_{DD\_HV\_OSC}$ = 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

Table 12. PLL1 electrical characteristics[1]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{PLL0IN}	SR	PLL1 input clock	—	38	—	78	MHz
f_{CLK_PFD}	CC	PFD input clock frequency	—	19	—	39	MHz
$f_{PLL0VCO}$	CC	PLL1 VCO frequency	—	600	—	1250	MHz
$t_{PLL0LOCK}$	CC	PLL1 lock time	—	—	—	100	µs
$\lvert\Delta_{PLL0PHISPJ}\rvert$	CC	PLL1 period jitter	f_{VCO}= 800 MHz	—	50	200	ps
D_{TC}	CC	Output duty cycle		45	50	55	%

1 $V_{DD\_HV\_OSC}$ = 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

Table 13. External Oscillator electrical specifications[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
f_{XTAL}	CC	Crystal Frequency Range[2]	—	4	8	MHz
			—	>8	20	
			—	>20	40	
t_{cst}	CC	Crystal start-up time [3,4]	T_J = 150 °C	—	5	ms
t_{rec}	CC	Crystal recovery time[5]	—	—	0.5	ms
V_{IHEXT}	CC	EXTAL input high voltage[6,7] (External Clock Input)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$	V_{REF} + 0.6	—	V
V_{ILEXT}	CC	EXTAL input low voltage[6,7] (External Clock Input)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$	—	V_{REF} - 0.6	V
C_{S_xtal}	CC	Total on-chip stray capacitance on XTAL/EXTAL pins[8]	BGA416, BGA512	8	8.6	pF
V_{EXTAL}	CC	Oscillation Amplitude on the EXTAL pin after startup[9]	T_J = –40 °C to 150 °C	0.5	1.6	V
V_{HYS}	CC	Comparator Hysteresis	T_J = –40 °C to 150 °C	0.1	1.0	V
I_{XTAL}	CC	XTAL current[13,10]	T_J = –40 °C to 150 °C	—	14	mA

1 All oscillator specifications are valid for VDD_HV_OSC = 4.5 V – 5.5 V.

3.8 ADC specifications

Table 14. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	D	Input leakage current	T_A = −40 °C	No current injection on adjacent pin	—	1	70	nA
		D		T_A = 25 °C		—	1	70	
		D		T_A = 85 °C			3	100	
		D		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 15. SARADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{AINx}	SR	—	Analog input voltage[3]	—	$V_{SS\_HV\_ADR}$	—	$V_{DD\_HV\_ADR}$	V
$V_{SS\_HV\_ADR}$	SR	—	Voltage on VSS_HV_ADR (ADC reference) pin with respect to ground (V_{SS_LV})[2]	—	–0.1	—	0.1	V
$V_{DD\_HV\_ADR}$	SR	—	Voltage on VDD_HV_ADR pin (ADC reference) with respect to ground (V_{SS_LV})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V
I_{ADCpwd}	SR	—	ADC consumption in power down mode	—	—	—	50	µA
I_{ADCrun}	SR	—	ADC consumption in running mode	—	—	—	6	mA
				$V_{DD\_HV\_ADV}$ = 5 V	3.33	—	32 + 4%	MHz
t_{ADC_PU}	SR	—	ADC power up delay	—	—	—	1.5	µs
t_{ADC_S}	CC	T	Sampling time[4] $V_{DD\_HV\_ADV}$ = 5 V	f_{ADC} = 20 MHz, INPSAMP = 12	600	—	—	ns
			Sampling time[4] $V_{DD\_HV\_ADV}$ = 5 V	f_{ADC} = 32 MHz, INPSAMP = 17	500	—	—	
			Sampling time[4] $V_{DD\_HV\_ADV}$ = 5 V	f_{ADC} = 3.33 MHz, INPSAMP = 255	—	—	76.2	µs
			Sampling time[4] $V_{DD\_HV\_ADV}$ = 5 V	f_{ADC} = 3.33 MHz, INPSAMP = 255	—	—	76.2	
t_{ADC_C}	CC	P	Conversion time[5] $V_{DD\_HV\_ADV}$ = 5 V	f_{ADC} = 20 MHz, INPCMP = 0	2.4	—	—	µs
			Conversion time[5] $V_{DD\_HV\_ADV}$ = 5 V	f_{ADC} = 32 MHz, INPCMP = 0	1.5	—	—	µs

			Conversion time[5] $V_{DD\_HV\_ADV}$ = 5 V	$f_{ADC\ 1}$ = 13.33 MHz, INPCMP = 0	—	—	3.6	µs
			Conversion time[5,] $V_{DD\_HV\_ADV}$ = 5 V	f_{ADC1} = 13.33 MHz, INPCMP = 0	—	—	3.6	µs
Δ_{ADC_SYS}	SR	—	ADC digital clock duty cycle	ADCLKSEL = 1[6]	45	—	55	%
C_S	CC	D	ADC input sampling capacitance	—	—	—	5	pF
C_{P1}	CC	D	ADC_1 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_1 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_1 input pin capacitance 3	—	—	—	1.5	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—	—	—	0.3	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC_1 input, different from the converted one, $V_{DD\_HV\_ADR}$ = 5.0 V ± 10%	–5	—	5	mA
| INLP |	CC	T	Absolute integral nonlinearity – Precise channels	No overload	—	1	3	LSB
| INLX |	CC	T	Absolute integral nonlinearity – Extended channels	No overload	—	1.5	5	LSB
| DNL |	CC	T	Absolute differential nonlinearity	No overload	—	0.5	1	LSB
| E_O |	CC	T	Absolute offset error	—	—	2	—	LSB
| E_G |	CC	T	Absolute gain error	—	—	2	—	LSB
TUEP[7]	CC	P	Total unadjusted error for precise channels, input only pins	Without current injection	–6	—	6	LSB
		T		With current injection	–8	—	8	
TUEX[7]	CC	T	Total unadjusted error for extended channel	Without current injection	–10	—	10	LSB
				With current injection	–12	—	12	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

[2] Analog and digital V_{SS} **must** be common (to be tied together externally).

[3] V_{AINx} may exceed V_{SS_ADC1} and V_{DD_ADC1} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.

[4] During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC1_S}. After the end of the sampling time t_{ADC1_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sampling clock t_{ADC1_S} depend on programming.

[5] This parameter does not include the sampling time t_{ADC1_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

[6] Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

[7] Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

3.9 Power management: PMC, POR/LVD, sequencing

3.9.1 Power management electrical characteristics

The power management module monitors the different power supplies. It also generates the internal supplies that are required for correct device functionality. The power management is supplied by the $V_{DD\_HV\_PMC}$ supply (see Table 8).

3.9.2 Power management integration

In order to ensure correct functionality of the device, it is recommended to follow below integration scheme.

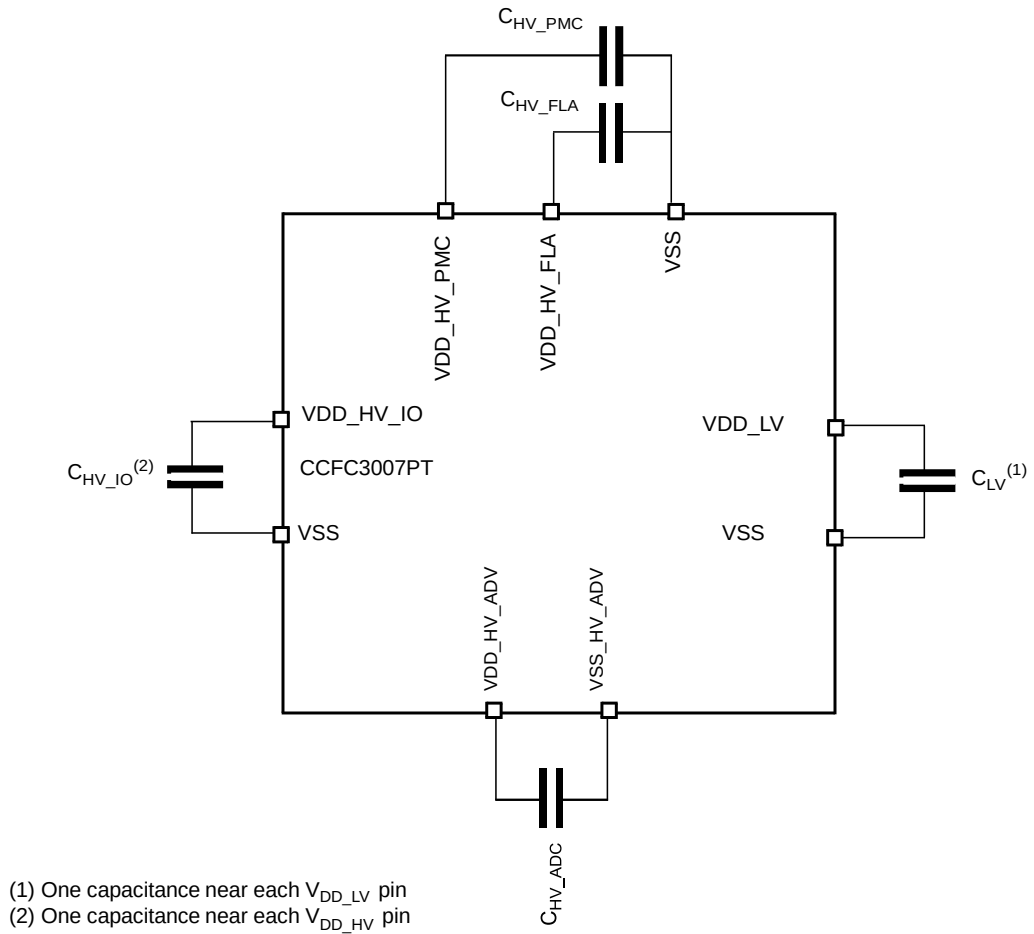


Figure 6. Recommended supply pin circuits

The following table describes the supply stability capacitances required on the device for proper operation.

Table 16. Device power supply integration

Symbol		Parameter		Conditions	Value[1]			Unit
					Min	Typ	Max	
C_{LV}	SR	Minimum VDD_LV external capacitance [2]	Bulk capacitance	External regulator bandwidth > 20 KHz	10	—	—	µF
			Total bypass capacitance at external pin		See Note 3	—	—	
C_{HV_IO}	SR	Minimum VDD_HV_IO external capacitance		—	4.7	—	—	µF
C_{HV_FLA}	SR	Minimum VDD_HV_FLA external capacitance [4]		—	0.75	1.0	—	µF
C_{HV_PMC}	SR	Minimum $V_{DD\_HV\_PMC}$ External Capacitance [5 6]			2.2	4.7	—	µF
C_{HV_ADC}	SR	Minimum $V_{DD\_HV\_ADV}$ external capacitance[8]			1.5	3.3	—	µF

1 See Figure 6 for capacitor integration.
2 Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over voltage, temperature, and aging.
3 Each VDD_LV pin requires both a 0.1µF and 0.01µF capacitor for high-frequency bypass and EMC requirements.
4 The typical CHV_FLA bulk capacitance value is 1uF.
5 For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between VDD_HV_PMC and VSS_HV.
6 VDD_HV_PMC is shorted to VDD_HV_IO_MAIN.
7 For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between VDD_HV_ADV and VSS_HV_ADV.

3.9.3 3.3V flash supply

Table 17. Flash power supply

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
[1]	CC	Flash regulator DC output voltage	Before trimming	3.0	3.3	3.5	V
			After trimming –40°C ≤ T_J ≤ 25°C	TBD	3.3	TBD	

1 Min value accounts for all static and dynamic variations of the regulator (min cap as 0.75uF).

3.10 AC specifications

All AC timing specifications are valid up to 150 ℃, except where explicitly noted.

3.10.1 Debug and calibration interface timing

3.10.1.1 JTAG interface timing

Table 18. JTAG pin AC electrical characteristics[1,2]

#	Symbol		Characteristic	Value		Unit
				Min	Max	
1	t_{JCYC}	CC	TCK cycle time	100	—	ns
2	t_{JDC}	CC	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	CC	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	CC	TCK low to TDO data valid	—	16[3]	ns
7	t_{TDOI}	CC	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	CC	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	CC	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	CC	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	CC	TCK falling edge to output valid	—	600[4]	ns
12	t_{BSDVZ}	CC	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	CC	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	CC	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	CC	TCK rising edge to boundary scan input invalid	15	—	ns

1 These specifications apply to JTAG boundary scan only. See Table 18 for functional specifications.

2 JTAG timing specified at $V_{DD\_HV\_IO\_MAIN}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.

3 Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.

[4] Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

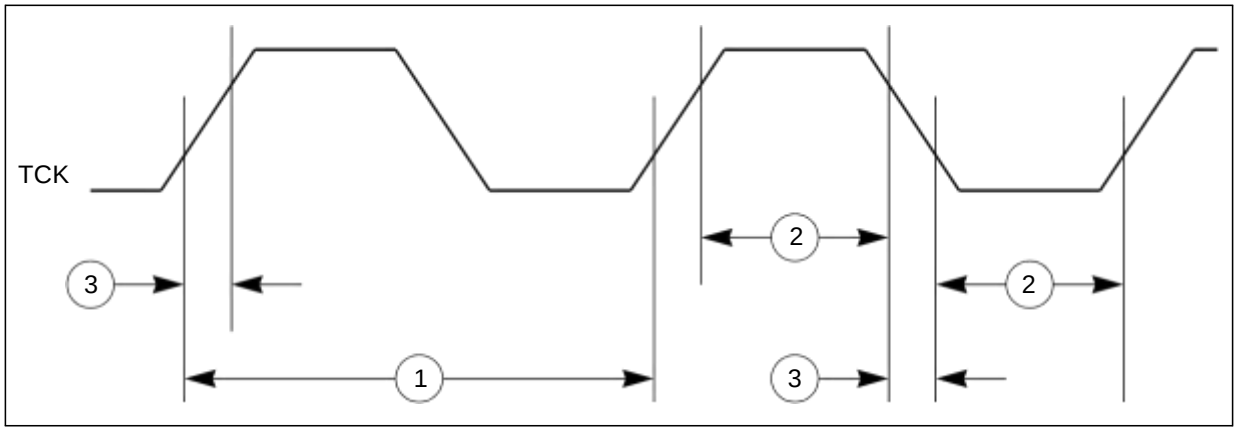


Figure 7. JTAG test clock input timing

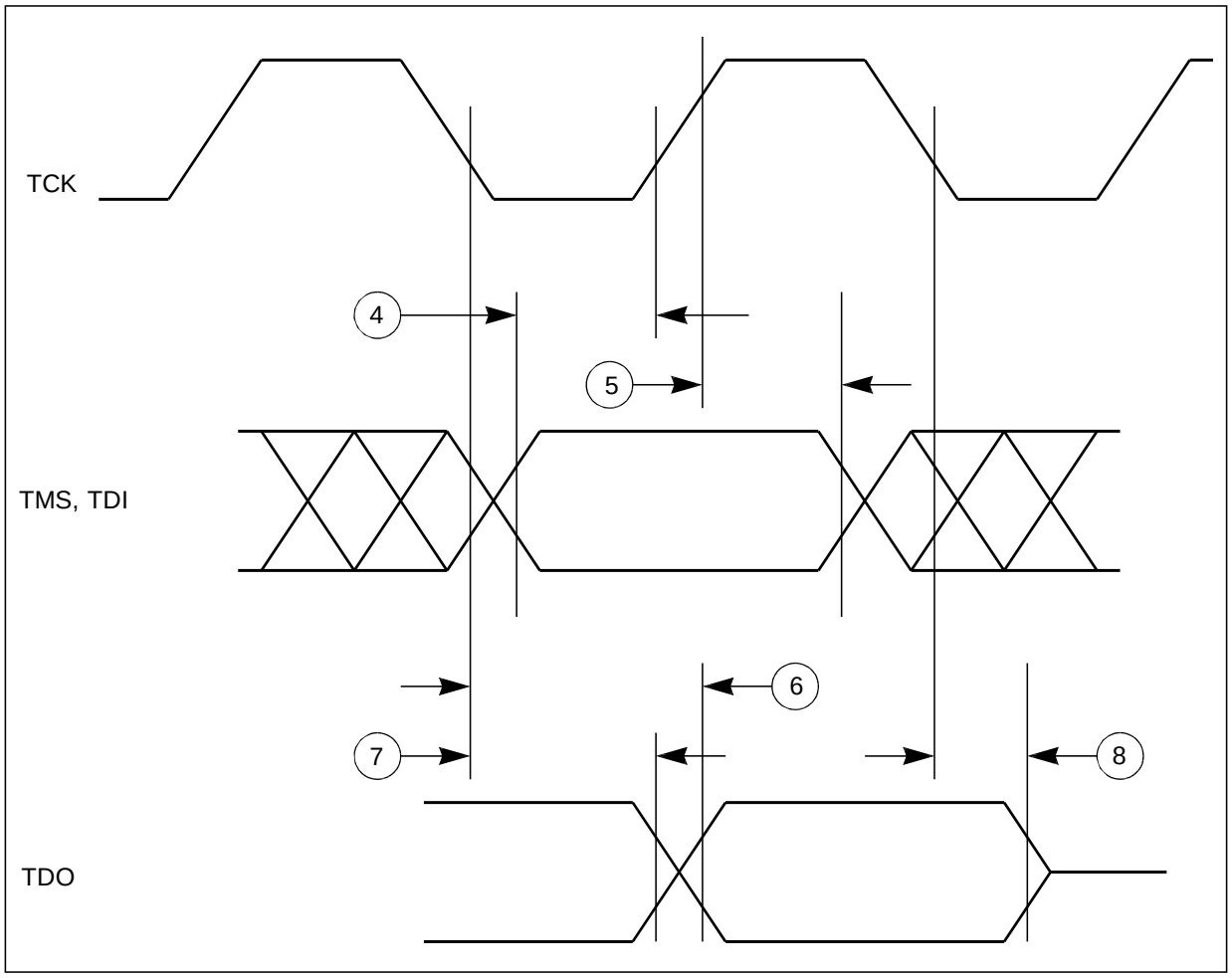


Figure8. JTAG test access port timing

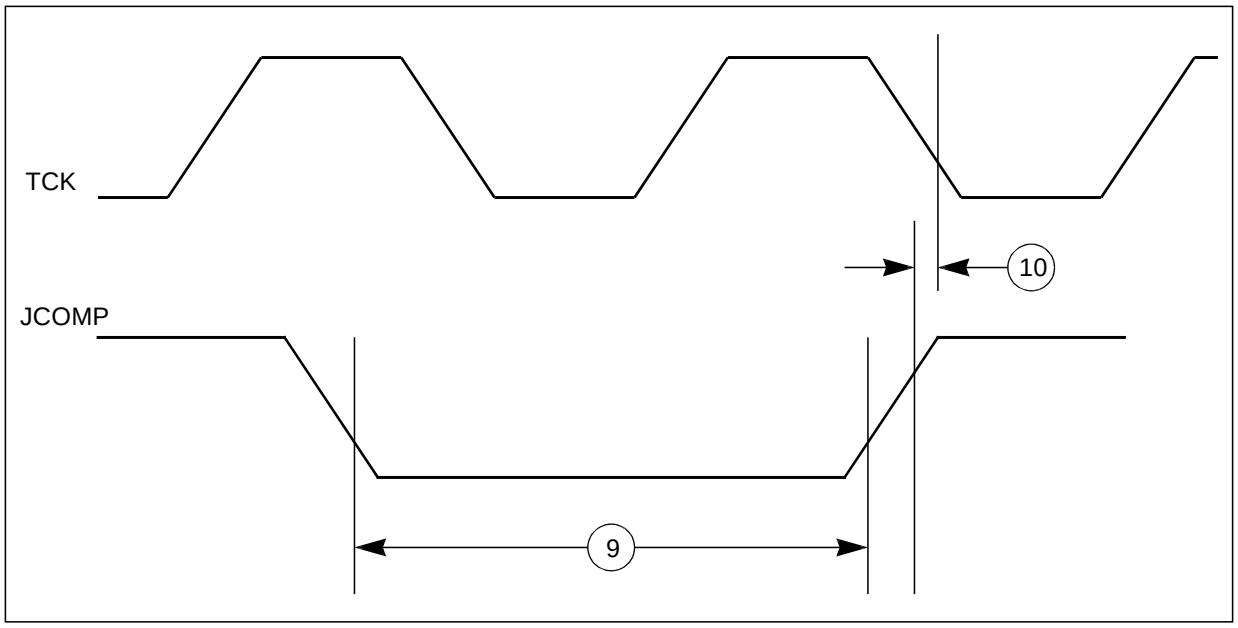


Figure 9. JTAG JCOMP timing

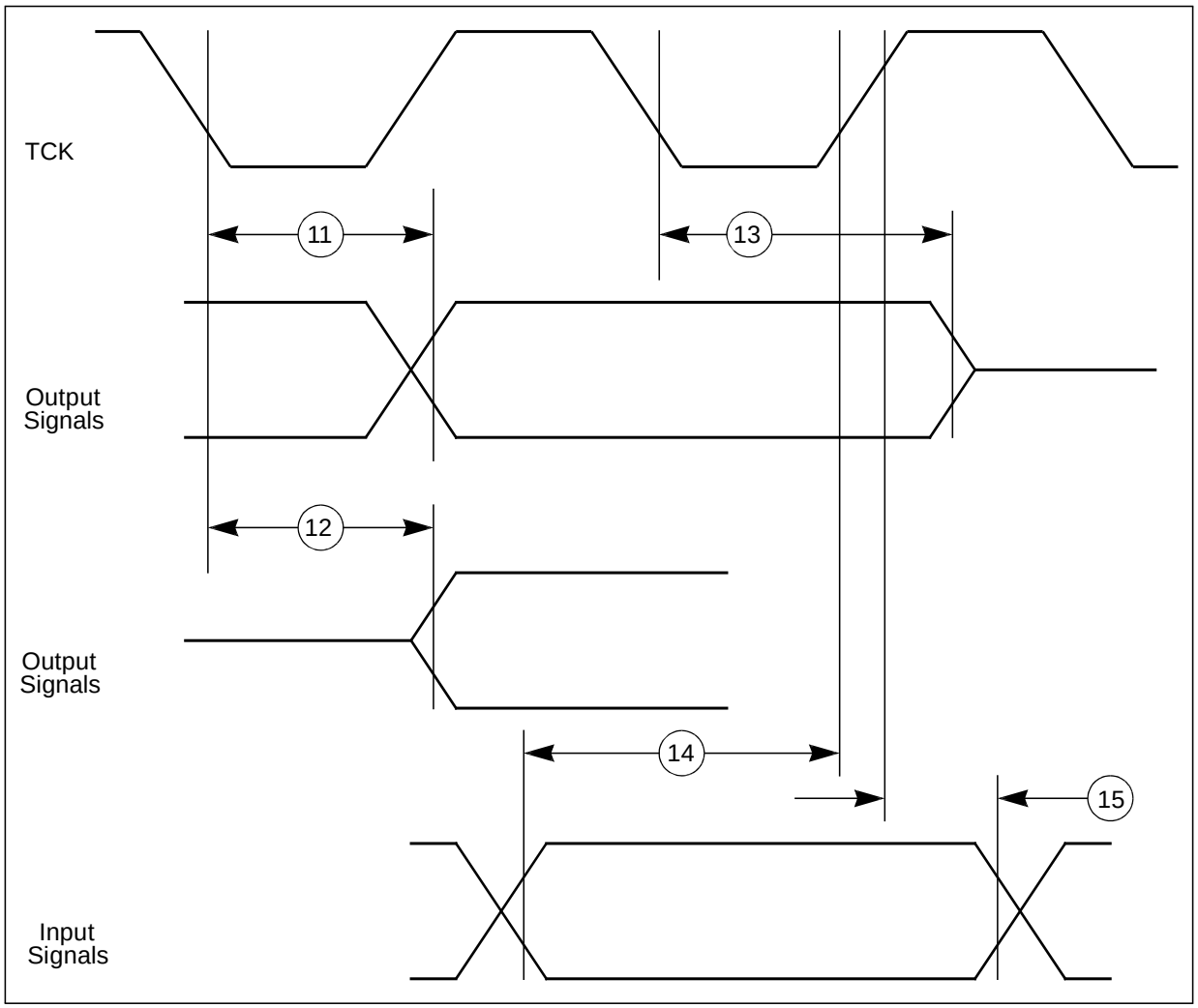


Figure 10. JTAG boundary scan timing

3.10.2 DSPI timing with CMOS and LVDS[1] pads

DSPI channel frequency support is shown in Table 50. Timing specifications are shown in Table 51, Table 52, Table 54, Table 55 and Table 56.

Table 50. DSPI channel frequency support

DSPI use mode		Max usable frequency (MHz)[1,2]
CMOS (Master mode)	Full duplex – Classic timing (Table 19)	17
	Full duplex – Modified timing (Table 20)	30
	Output only mode (SCK/SOUT/PCS) (Table 19 and Table 20)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 24)	30
LVDS (Master mode)[3]	Full duplex – Modified timing (Table 22)	33
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 23)	40

1 Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
2 Maximum usable frequency does not take into account external device propagation delay.
3 µS Channel and LVDS timing is not supported for DSPI12.

3.10.2.1 DSPI master mode full duplex timing with CMOS and LVDS pads

3.10.2.1.1 DSPI CMOS Master Mode – Classic Timing

Table 19. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	SCK cycle time	SCK drive strength				
				PAD3V5V = 0	25 pF	33.0	—	ns
				PAD3V5V = 0	50 pF	80.0	—	
2	t_{CSC}	CC	PCS to SCK delay	SCK and PCS drive strength				
				PAD3V5V = 0	25 pF	[5]	—	ns
				PAD3V5V = 0	50 pF	$(N^4 \times t_{SYS}^5) - 16$	—	

1. DSPI in TSB mode with LVDS pads can be used to implement Micro Second Channel bus protocol.

Table 19. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
3	t_{ASC}	CC	After SCK delay	SCK and PCS drive strength				
				PAD3V5V = 0	PCS = 0 pF SCK = 50 pF	($M^6 \times t_{SYS}^5$) – 35	—	ns
				PAD3V5V = 0	PCS = 0 pF SCK = 50 pF	($M^6 \times t_{SYS}^5$) – 35	—	
4	t_{SDC}	CC	SCK duty cycle[7]	SCK drive strength				
				PAD3V5V = 0	0 pF	$^1/_2t_{SCK}$ – 2	$^1/_2t_{SCK}$ + 2	ns
				PAD3V5V = 0	0 pF	$^1/_2t_{SCK}$ – 2	$^1/_2t_{SCK}$ + 2	
PCS strobe timing								
5	t_{PCSC}	CC	PCSx to PCSS time[8]	PCS and PCSS drive strength				
				PAD3V5V = 0	25 pF	16.0	—	ns
6	t_{PASC}	CC	PCSS to PCSx time[8]	PCS and PCSS drive strength				
				PAD3V5V = 0	25 pF	16.0	—	ns
SIN setup time								
7	t_{SUI}	CC	SIN setup time to SCK[9]	SCK drive strength				
				PAD3V5V = 0	25 pF	25.0	—	ns
				PAD3V5V = 0	50 pF	32.75	—	
SIN hold time								
8	t_{HI}	CC	SIN hold time from SCK[9]	SCK drive strength				
				PAD3V5V = 0	0 pF	–1.0	—	ns
				PAD3V5V = 0	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	SOUT data valid time from SCK[10]	SOUT and SCK drive strength				
				PAD3V5V = 0	25 pF	—	7.0	ns
				PAD3V5V = 0	50 pF	—	8.0	
SOUT data hold time (after SCK edge)								

Table 19. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
10	t_{HO}	CC	SOUT data hold time after SCK[10]	SOUT and SCK drive strength				
				PAD3V5V = 0	25 pF	–7.7	—	ns
				PAD3V5V = 0	50 pF	–11.0	—	

1 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

2 All timing values for output signals in this table are measured to 50% of the output voltage.

3 Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.

4 N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

5 t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).

6 M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

7 t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.

8 PCSx and PCSS using same pad configuration.

9 Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.

10 SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

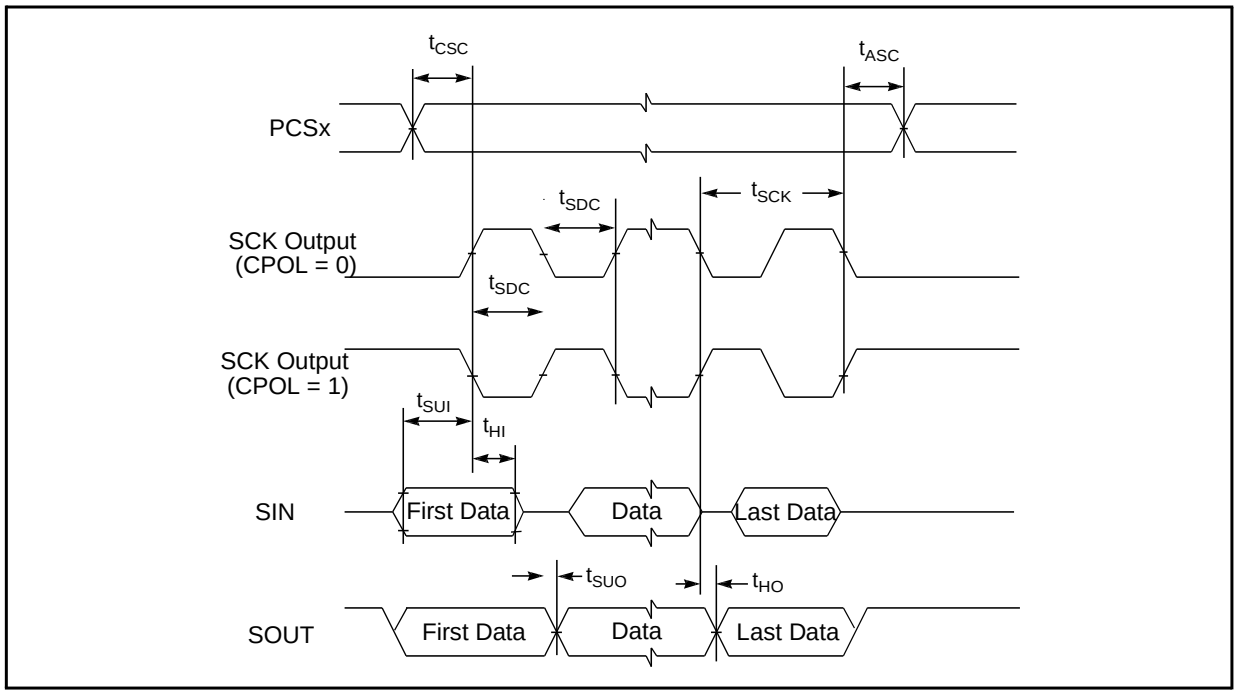


Figure 11. DSPI CMOS master mode – classic timing, CPHA = 0

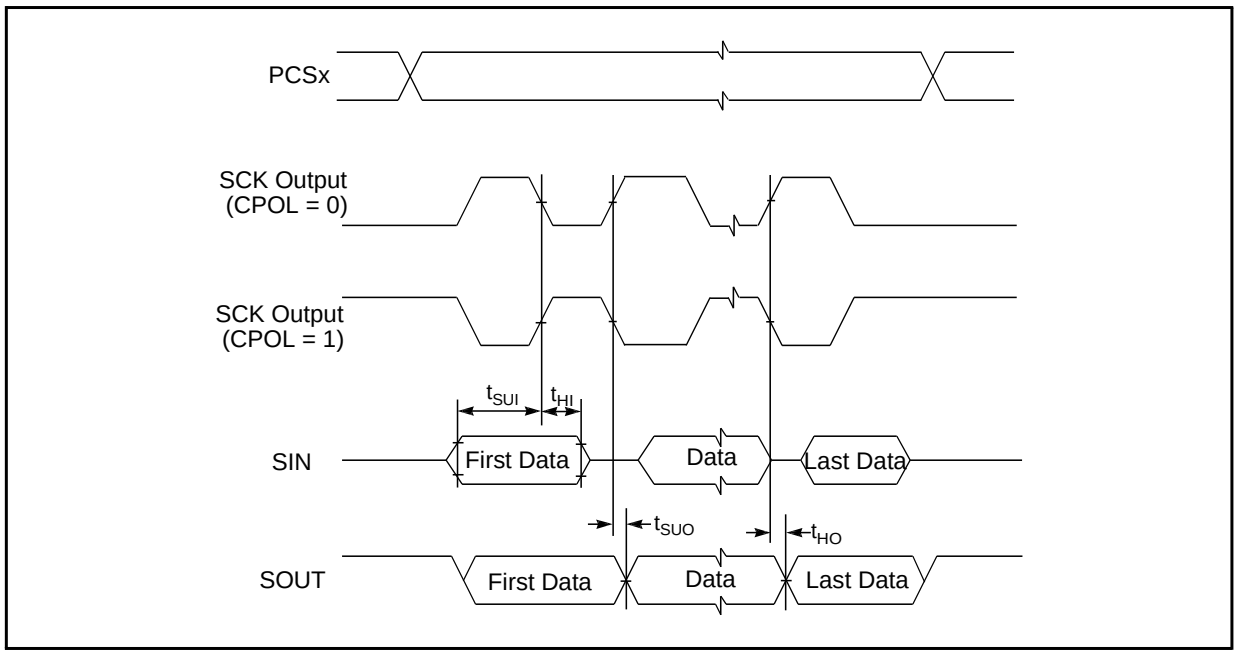


Figure 12. DSPI CMOS master mode – classic timing, CPHA = 1

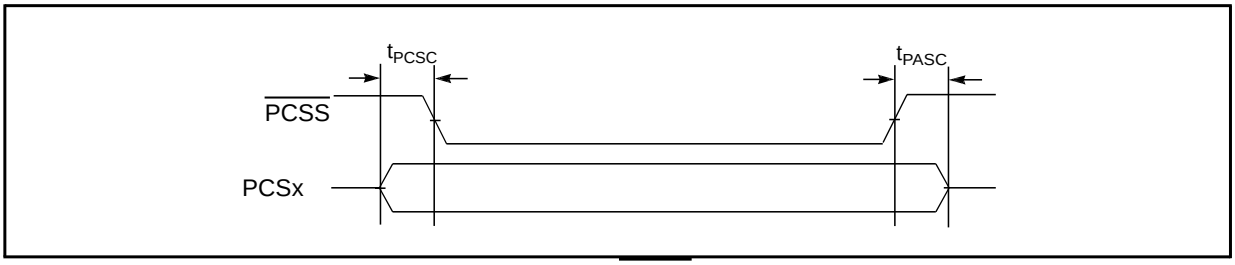


Figure 13. DSPI PCS strobe (PCSS) timing (master mode)

3.10.2.1.2 DSPI CMOS Master Mode – Modified Timing

Table 20. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	SCK cycle time	SCK drive strength				
				PAD3V5V = 0	25 pF	33.0	—	ns
				PAD3V5V = 0	50 pF	80.0	—	
2	t_{CSC}	CC	PCS to SCK delay	SCK and PCS drive strength				
				PAD3V5V = 0	25 pF	$(N^4 \times t_{SYS}^5) - 16$	—	ns
				PAD3V5V = 0	50 pF	$(N^4 \times t_{SYS}^5) - 16$	—	
3	t_{ASC}	CC	After SCK delay	SCK and PCS drive strength				
				PAD3V5V = 0	PCS = 0 pF SCK = 50 pF	$(M^6 \times t_{SYS}^5) - 35$	—	ns
				PAD3V5V = 0	PCS = 0 pF SCK = 50 pF	$(M^6 \times t_{SYS}^5) - 35$	—	
4	t_{SDC}	CC	SCK duty cycle[7]	SCK drive strength				
				PAD3V5V = 0	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
				PAD3V5V = 0	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
PCS strobe timing								

Table 20. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
5	t_{PCSC}	CC	PCSx to PCSS time[8]	PCS and PCSS drive strength				
				PAD3V5V = 0	25 pF	16.0	—	ns
6	t_{PASC}	CC	PCSS to PCSx time[8]	PCS and PCSS drive strength				
				PAD3V5V = 0	25 pF	16.0	—	ns
SIN setup time								
7	t_{SUI}	CC	SIN setup time to SCK CPHA = 0[9]	SCK drive strength				
				PAD3V5V = 0	25 pF	25 – (P^{10} × t_{SYS}[5])	—	ns
				PAD3V5V = 0	50 pF	32.75 – (P^{10} × t_{SYS}[5])	—	
			SIN setup time to SCK CPHA = 1[9]	SCK drive strength				
				PAD3V5V = 0	25 pF	25.0	—	ns
				PAD3V5V = 0	50 pF	32.75	—	
SIN hold time								
8	t_{HI}	CC	SIN hold time from SCK CPHA = 0[9]	SCK drive strength				
				PAD3V5V = 0	0 pF	–1 + (P^{9} × t_{SYS}[4])	—	ns
				PAD3V5V = 0	0 pF	–1 + (P^{9} × t_{SYS}[4])	—	
			SIN hold time from SCK CPHA = 1[9]	SCK drive strength				
				PAD3V5V = 0	0 pF	–1.0	—	ns
				PAD3V5V = 0	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	SOUT data valid time from SCK CPHA = 0[10]	SOUT and SCK drive strength				
				PAD3V5V = 0	25 pF	—	7.0 + t_{SYS}[5]	ns
				PAD3V5V = 0	50 pF	—	8.0 + t_{SYS}[5]	
			SOUT data valid time from SCK CPHA = 1[10]	SOUT and SCK drive strength				
				PAD3V5V = 0	25 pF	—	7.0	ns
				PAD3V5V = 0	50 pF	—	8.0	
SOUT data hold time (after SCK edge)								

Table 20. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
10	t_{HO}	CC	SOUT data hold time after SCK CPHA = 0[11]	SOUT and SCK drive strength				
				PAD3V5V = 0	25 pF	–7.7 + t_{SYS}[5]	—	ns
				PAD3V5V = 0	50 pF	–11.0 + t_{SYS}[5]	—	
			SOUT data hold time after SCK CPHA = 1[11]	SOUT and SCK drive strength				
				PAD3V5V = 0	25 pF	–7.7	—	ns
				PAD3V5V = 0	50 pF	–11.0	—	

1 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

2 All timing values for output signals in this table are measured to 50% of the output voltage.

3 Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.

4 N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

5 t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).

6 M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

7 t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.

8 PCSx and PCSS using same pad configuration.

9 Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.

10 P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

11 SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

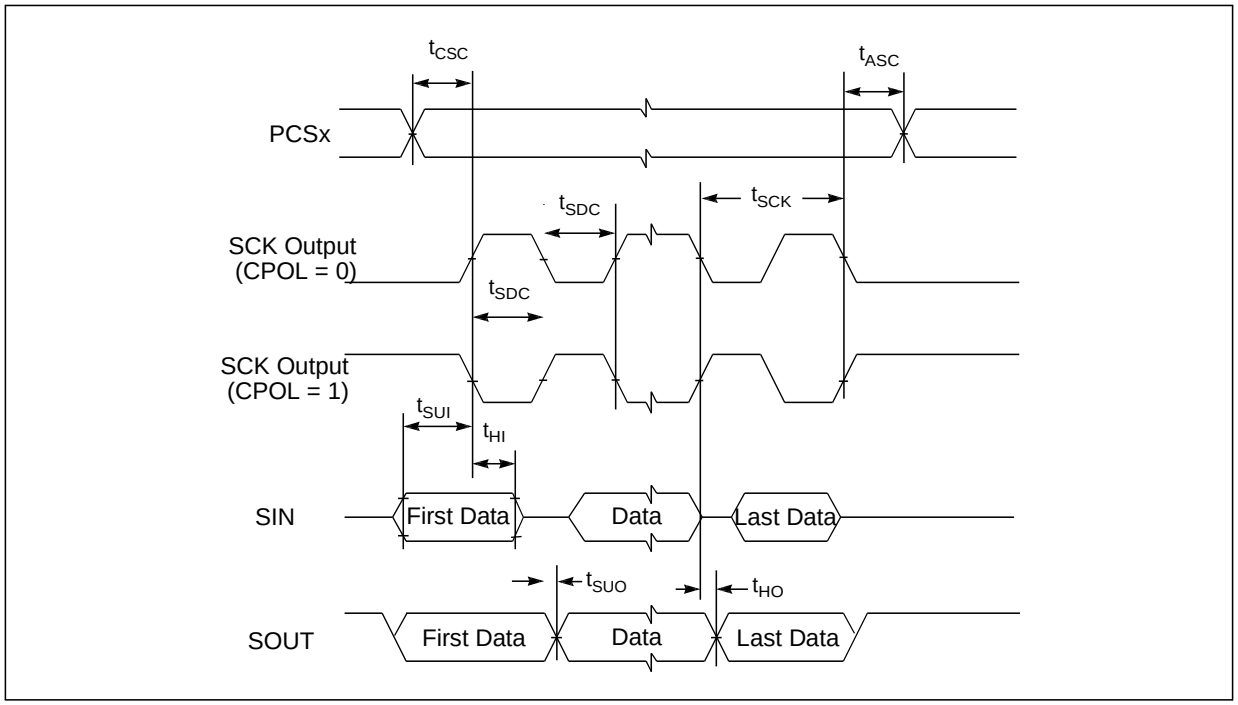


Figure 14. DSPI CMOS master mode – modified timing, CPHA = 0

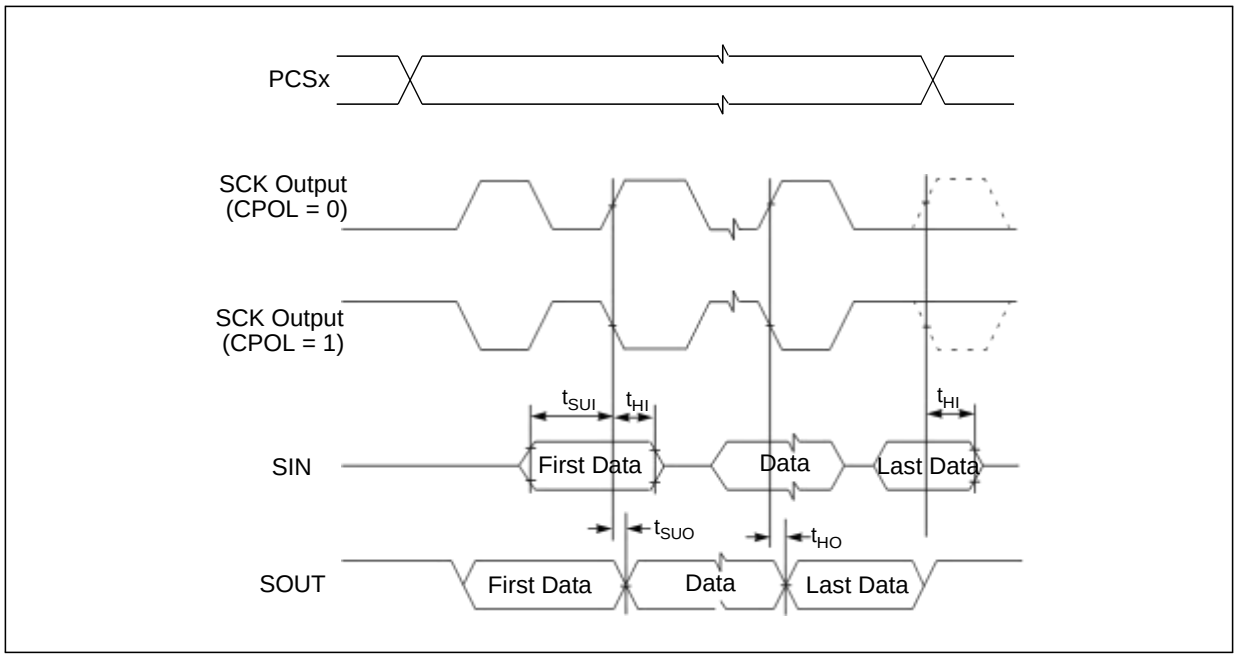


Figure 15. DSPI CMOS master mode – modified timing, CPHA = 1

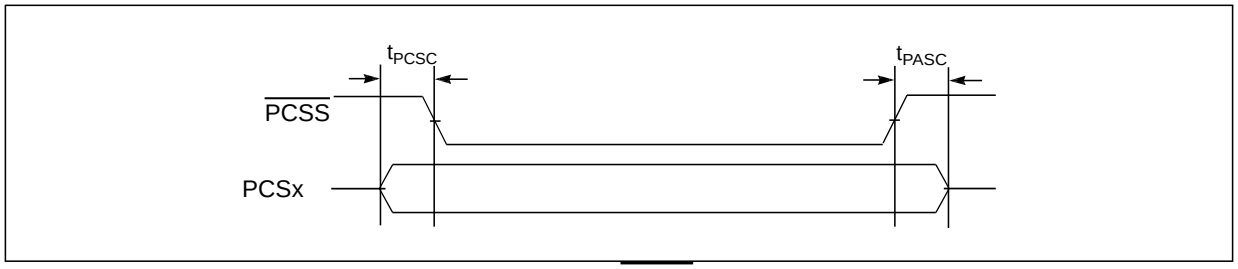


Figure 16. DSPI PCS strobe (PCSS) timing (master mode)

3.10.2.1.3 DSPI LVDS Master Mode – Modified Timing

Table 21. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1

#	Symbol		Characteristic	Condition		Value[1]		Unit
				Pad drive	Load	Min	Max	
1	t_{SCK}	CC	SCK cycle time	LVDS	15 pF to 25 pF differential	30.0	—	ns
2	t_{CSC}	CC	PCS to SCK delay (LVDS SCK)	PCS drive strength				
				PAD3V5V = 0	25 pF	$(N^2 \times t_{SYS}^3) - 10$	—	ns
				PAD3V5V = 0	50 pF	$(N^2 \times t_{SYS}^3) - 10$	—	ns
3	t_{ASC}	CC	After SCK delay (LVDS SCK)	PAD3V5V = 0	PCS = 0 pF SCK = 25 pF	$(M^4 \times t_{SYS}^3) - 8$	—	ns
				PAD3V5V = 0	PCS = 0 pF SCK = 25 pF	$(M^4 \times t_{SYS}^3) - 8$	—	ns
4	t_{SDC}	CC	SCK duty cycle[5]	LVDS	15 pF to 25 pF differential	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	ns
7	t_{SUI}	CC	SIN setup time					
			SIN setup time to SCK CPHA = 0[6]	SCK drive strength				
				LVDS	15 pF to 25 pF differential	$23 - (P^7 \times t_{SYS}^3)$	—	ns
			SIN setup time to SCK CPHA = 1[6]	SCK drive strength				
				LVDS	15 pF to 25 pF differential	23	—	ns

Table 21. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1

#	Symbol		Characteristic	Condition		Value[1]		Unit
				Pad drive	Load	Min	Max	
8	t_{HI}	CC	SIN Hold Time					
			SIN hold time from SCK CPHA = 0[6]	SCK drive strength				
				LVDS	0 pF differential	–1 + ($P^7 \times t_{SYS}^3$)	—	ns
			SIN hold time from SCK CPHA = 1[6]	SCK drive strength				
				LVDS	0 pF differential	–1	—	ns
9	t_{SUO}	CC	SOUT data valid time (after SCK edge)					
			SOUT data valid time from SCK CPHA = 0[8]	SOUT and SCK drive strength				
				LVDS	15 pF to 25 pF differential	—	7.0 + t_{SYS}^3	ns
			SOUT data valid time from SCK CPHA = 1[8]	SOUT and SCK drive strength				
				LVDS	15 pF to 25 pF differential	—	7.0	ns
10	t_{HO}	CC	SOUT data hold time (after SCK edge)					
			SOUT data hold time after SCK CPHA = 0[8]	SOUT and SCK drive strength				
				LVDS	15 pF to 25 pF differential	–7.5 + t_{SYS}^3	—	ns
			SOUT data hold time after SCK CPHA = 1[8]	SOUT and SCK drive strength				
				LVDS	15 pF to 25 pF differential	–7.5	—	ns

1 All timing values for output signals in this table are measured to 50% of the output voltage.

2 N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

3 t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).

4 M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

5 t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.

6 Input timing assumes an input slew rate of 1 ns (10% – 90%) and LVDS differential voltage = ±100 mV.

7 P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

[8] SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 22. DSPI LVDS slave timing – full duplex – modified transfer format (MTFE = 0/1)[1]

#	Symbol		Characteristic	Condition		Value		Unit
				Pad drive	Load	Min	Max	
1	t_{SCK}	CC	SCK cycle time[2]	—	—	62	—	ns
2	t_{CSC}	SR	SS to SCK delay[2]	—	—	16	—	ns
3	t_{ASC}	SR	SCK to SS delay[2]	—	—	16	—	ns
4	t_{SDC}	CC	SCK duty cycle[2]	—	—	30	—	ns
5	t_A	CC	Slave Access Time[2, 3, 4] (SS active to SOUT	PAD3V5V = 0	25 pF	—	50	ns
				PAD3V5V = 0	50 pF	—	50	ns
6	t_{DIS}	CC	Slave SOUT Disable Time [2, 3, 4](SS inactive to	PAD3V5V = 0	25 pF	—	5	ns
				PAD3V5V = 0	50 pF	—	5	ns
7	t_{SUI}	CC	~~Data~~ setup time for inputs[2]	—	—	10	—	ns
8	t_{HI}	CC	Data hold time for inputs[2]	—	—	10	—	ns
9	t_{SUO}	CC	SOUT Valid Time[2, 3, 4] (after SCK edge)	PAD3V5V = 0	25 pF	—	30	ns
				PAD3V5V = 0	50 pF	—	30	ns
10	t_{HO}	CC	SOUT Hold Time[2, 3, 4] (after SCK edge)	PAD3V5V = 0	25 pF	2.5	—	ns
				PAD3V5V = 0	50 pF	2.5	—	ns

[1] DSPI slave operation is only supported for a single master and single slave on the device. Timing is valid for that case only.

[2] Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL / Automotive voltage thresholds.

[3] All timing values for output signals in this table, are measured to 50% of the output voltage.

[4] All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

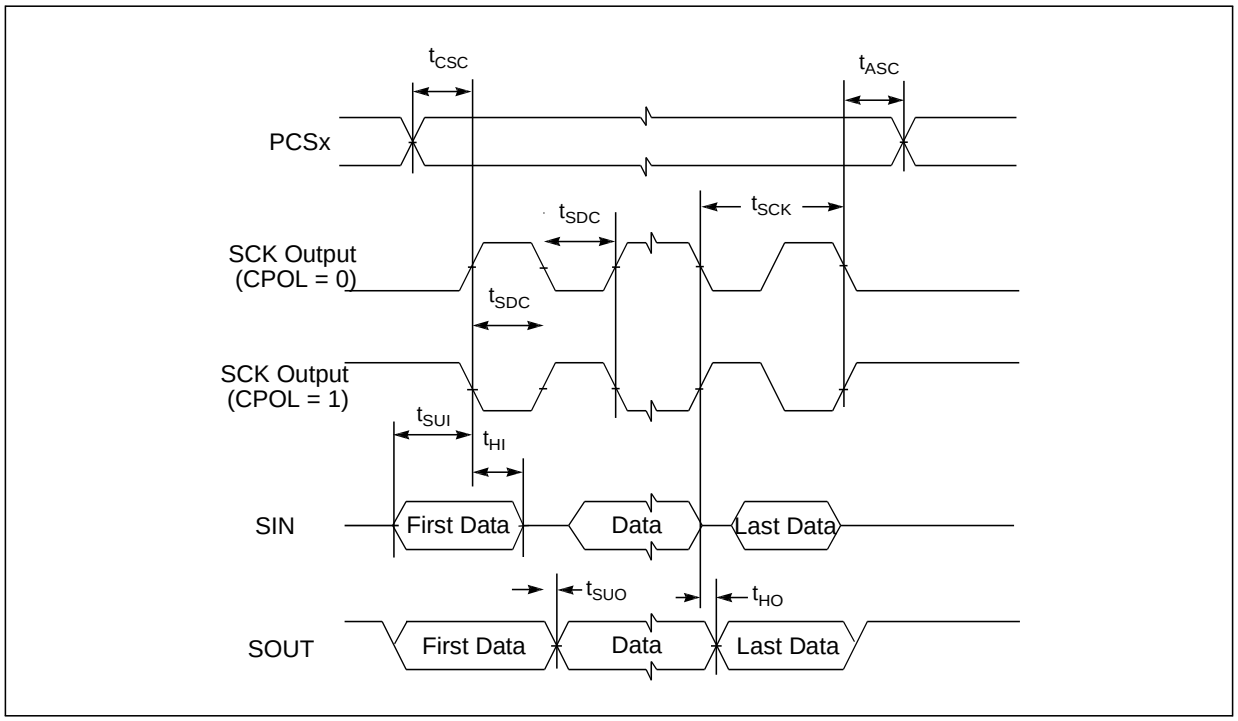


Figure 17. DSPI LVDS master mode – modified timing, CPHA = 0

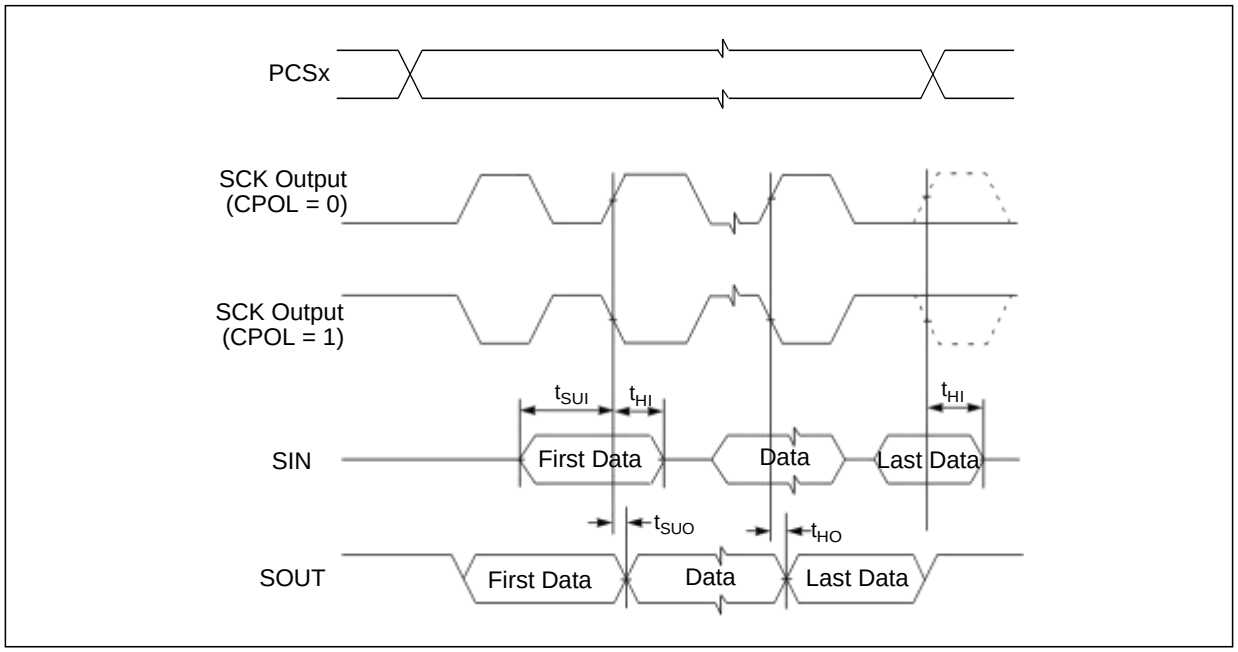


Figure 18. DSPI LVDS master mode – modified timing, CPHA = 1

3.10.2.1.4 DSPI Master Mode – Output Only

Table 23. DSPI LVDS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1,2]

#	Symbol		Characteristic	Condition		Value		Unit
				Pad drive	Load	Min	Max	
1	t_{SCK}	CC	SCK cycle time	LVDS	15 pF to 50 pF differential	25.0	—	ns
2	t_{CSV}	CC	PCS valid after SCK[3] (SCK with 50 pF differential load cap.)	PAD3V5V = 0	25 pF	—	6.0	ns
				PAD3V5V = 0	50 pF	—	10.5	ns
3	t_{CSH}	CC	PCS hold after SCK[3] (SCK with 50 pF differential load cap.)	PAD3V5V = 0	0 pF	–4.0	—	ns
				PAD3V5V = 0	0 pF	–4.0	—	ns
4	t_{SDC}	CC	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$^1/_2t_{SCK}$ – 2	$^1/_2t_{SCK}$ + 2	ns
SOUT data valid time (after SCK edge)								
5	t_{SUO}	CC	SOUT data valid time from SCK[4]	SOUT and SCK drive strength				
				LVDS	15 pF to 50 pF differential	—	3.5	ns
SOUT data hold time (after SCK edge)								
6	t_{HO}	CC	SOUT data hold time after SCK[4]	SOUT and SCK drive strength				
				LVDS	15 pF to 50 pF differential	–3.5	—	ns

1 All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.

2 TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.

3 With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.

4 SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 24. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1,2]

#	Symbol		Characteristic	Condition		Value[3]		Unit
				Pad drive[4]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	SCK cycle time	SCK drive strength				
				PAD3V5V = 0	25 pF	33.0	—	ns
				PAD3V5V = 0	50 pF	80.0	—	ns

Table 24. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1,2] (continued)

#	Symbol		Characteristic	Condition		Value[3]		Unit
				Pad drive[4]	Load (C_L)	Min	Max	
2	t_{CSV}	CC	PCS valid after SCK[5]	SCK and PCS drive strength				
				PAD3V5V = 0	25 pF	7	—	ns
				PAD3V5V = 0	50 pF	8	—	ns
3	t_{CSH}	CC	PCS hold after SCK[5]	SCK and PCS drive strength				
				PAD3V5V = 0	PCS = 0 pF SCK = 50 pF	–14	—	ns
				PAD3V5V = 0	PCS = 0 pF SCK = 50 pF	–14	—	ns
4	t_{SDC}	CC	SCK duty cycle[6]	SCK drive strength				
				PAD3V5V = 0	0 pF	$^1/_2t_{SCK}$ – 2	$^1/_2t_{SCK}$ + 2	ns
				PAD3V5V = 0	0 pF	$^1/_2t_{SCK}$ – 2	$^1/_2t_{SCK}$ + 2	ns
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	SOUT data valid time from SCK CPHA = 1[7]	SOUT and SCK drive strength				
				PAD3V5V = 0	25 pF	—	7.0	ns
				PAD3V5V = 0	50 pF	—	8.0	ns
SOUT data hold time (after SCK edge)								
10	t_{HO}	CC	SOUT data hold time after SCK CPHA = 1[7]	SOUT and SCK drive strength				
				PAD3V5V = 0	25 pF	–7.7	—	ns
				PAD3V5V = 0	50 pF	–11.0	—	ns

1 TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.

2 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

3 All timing values for output signals in this table are measured to 50% of the output voltage.

4 Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.

5 With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.

6 t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.

7 SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

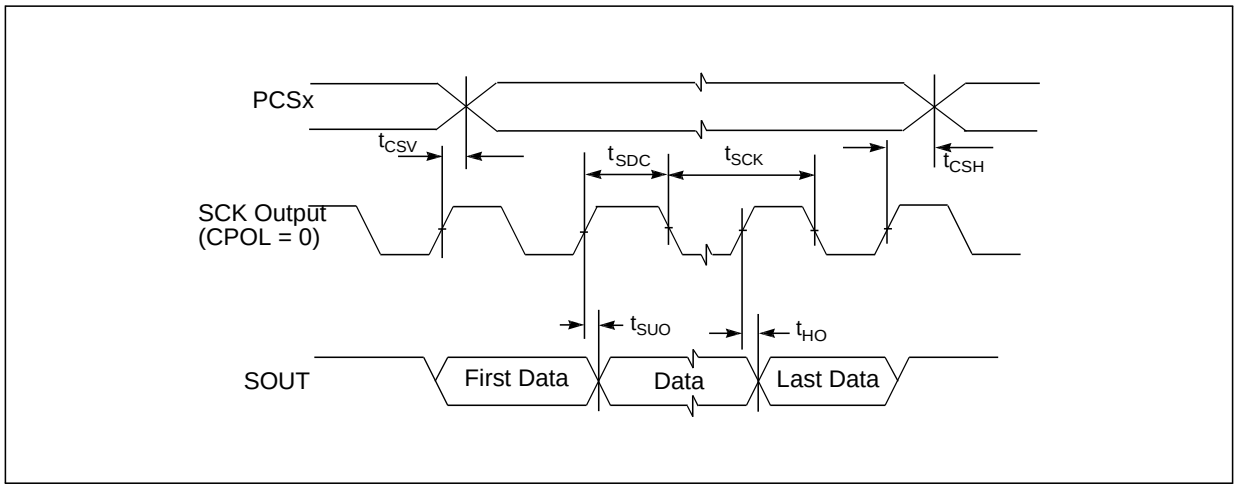


Figure 19. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1

3.10.2.2 Slave Mode timing

Table 25. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1)[1]

3

#	Symbol		Characteristic	Condition		Min	Max	Unit
				Pad Drive	Load			
1	t_{SCK}	CC	SCK Cycle Time[2]	-	-	62	—	ns
2	t_{CSC}	SR	SS to SCK Delay[2]	-	-	16	—	ns
3	t_{ASC}	SR	SCK to SS Delay[2]	-	-	16	—	ns
4	t_{SDC}	CC	SCK Duty Cycle[2]	-	-	30	—	ns
5	t_A	CC	Slave Access Time[2,3,4] (SS active to SOUT driven)	PAD3V5V = 0	25 pF	—	50	ns
				PAD3V5V = 0	50 pF	—	50	ns
6	t_{DIS}	CC	Slave SOUT Disable Time[2,3,4] (SS inactive to SOUT High-Z	PAD3V5V = 0	25 pF	—	5	ns
				PAD3V5V = 0	50 pF	—	5	ns
9	t_{SUI}	CC	Data Setup Time for Inputs[2]	—	—	10	—	ns
10	t_{HI}	CC	Data Hold Time for Inputs[2]	—	—	10	—	ns

Table 25. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1)[1]

#	Symbol		Characteristic	Condition		Min	Max	Unit
				Pad Drive	Load			
11	t_{SUO}	CC	SOUT Valid Time[2,3,4] (after SCK edge)	PAD3V5V = 0	25 pF	—	30	ns
				PAD3V5V = 0	50 pF	—	30	ns
12	t_{HO}	CC	SOUT Hold Time[2,3,4] (after SCK edge)	PAD3V5V = 0	25 pF	2.5	—	ns
				PAD3V5V = 0	50 pF	2.5	—	ns

1 DSPI slave operation is only supported for a single master and single slave on the device. Timing is valid for that case only.

2 Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL / Automotive voltage thresholds.

3 All timing values for output signals in this table, are measured to 50% of the output voltage.

4 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

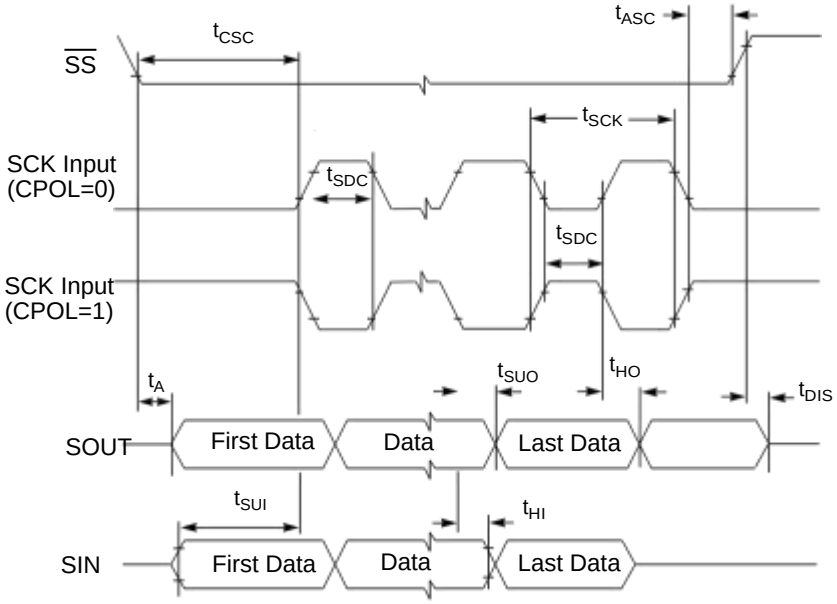


Figure 20. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 0

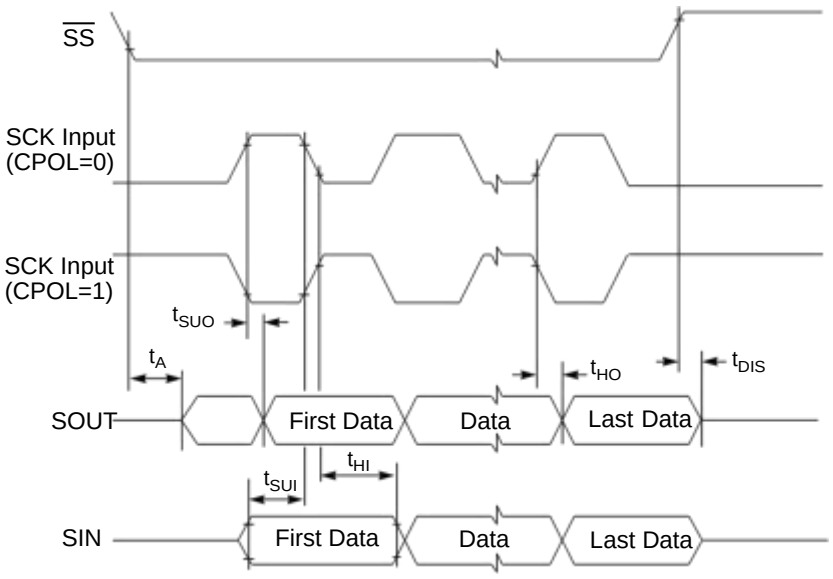


Figure 21. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 1

3.10.3 FEC timing

The FEC provides both MII and RMII interfaces in the 416 TEPBGA and 512 TEPBGA packages, and the MII and RMII signals can be configured for either CMOS or TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

3.10.3.1 MII receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Table 26. MII receive signal timing[1]

Symbol		Characteristic	Value		Unit
			Min	Max	
M1	CC	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	CC	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	CC	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	CC	RX_CLK pulse width low	35%	65%	RX_CLK period

[1] All timing specifications are referenced from RX_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.

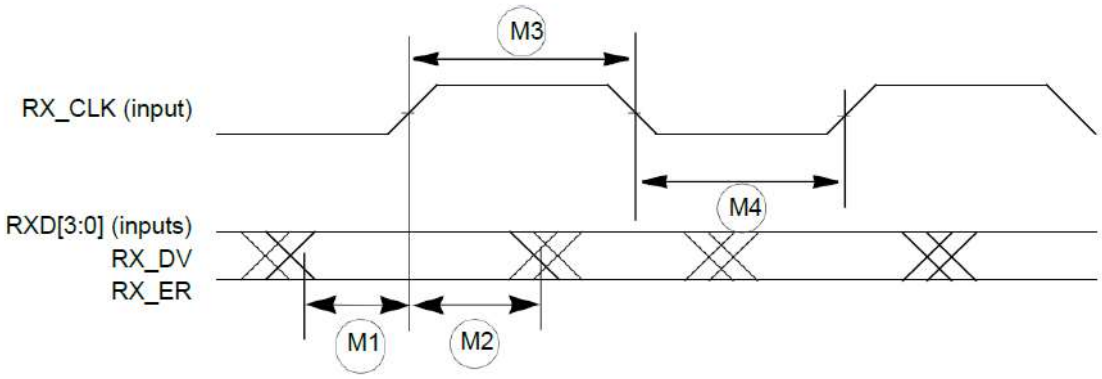


Figure 22. MII receive signal timing diagram

3.10.3.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the *CCFC3007PT Microcontroller Reference Manual's* Fast Ethernet Controller (FEC) chapter for details of this option and how to enable it.

Table 27. MII transmit signal timing[1]

Symbol		Characteristic	Value[2]		Unit
			Min	Max	
M5	CC	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	CC	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	CC	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	CC	TX_CLK pulse width low	35%	65%	TX_CLK period

1 All timing specifications are referenced from TX_CLK = 1.4 V to the valid output levels, 0.8 V and 2.0 V.

2 Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

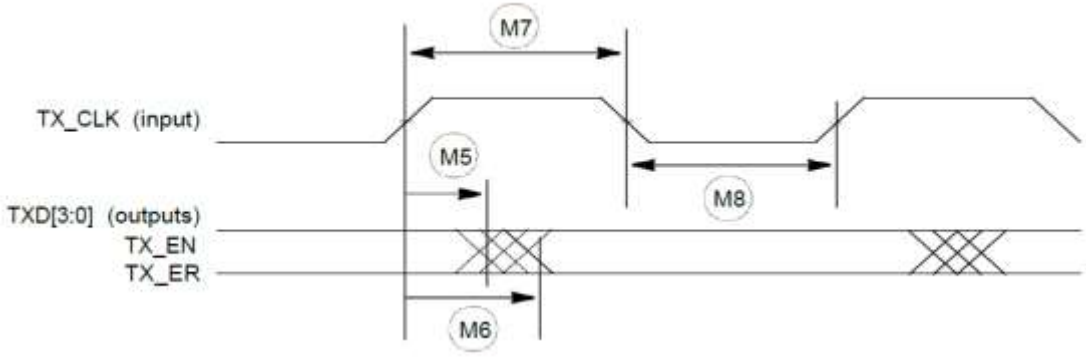


Figure 23. MII transmit signal timing diagram

3.10.3.3 MII async inputs signal timing (CRS and COL)

Table 28. MII async inputs signal timing

Symbol		Characteristic	Value		Unit
			Min	Max	
M9	CC	CRS, COL minimum pulse width	1.5	—	TX_CLK period

Figure 24. MII async inputs timing diagram

3.10.3.4 MII and RMII serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 29. MII serial management channel timing[1]

Symbol		Characteristic	Value[2]		Unit
			Min	Max	
M10	CC	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	CC	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	CC	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	MDIO (input) to MDC rising edge hold	0	—	ns
M14	CC	MDC pulse width high	40%	60%	MDC period
M15	CC	MDC pulse width low	40%	60%	MDC period

1 All timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

[2] Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

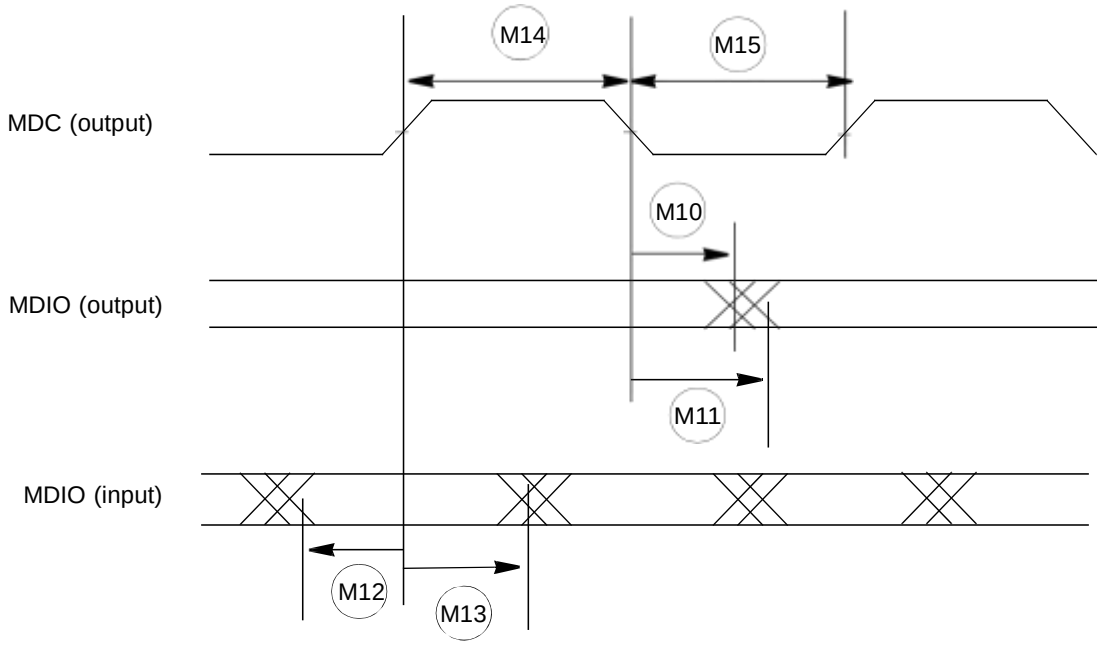


Figure 25. MII serial management channel timing diagram

3.10.3.5 RMII receive signal timing (RXD[1:0], CRS_DV)

The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Table 30. RMII receive signal timing[1]

Symbol		Characteristic	Value		Unit
			Min	Max	
R1	CC	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	CC	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	CC	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	CC	REF_CLK pulse width low	35%	65%	REF_CLK period

[1] All timing specifications are referenced from REF_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.

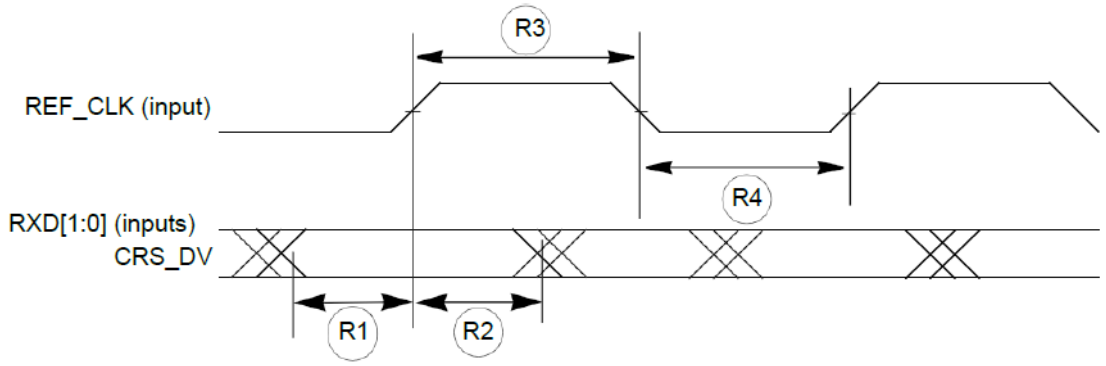


Figure 26. RMII receive signal timing diagram

3.10.3.6 RMII transmit signal timing (TXD[1:0], TX_EN)

The transmitter functions correctly up to a REF_CLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency, which is half that of the REF_CLK frequency.

The transmit outputs (TXD[1:0], TX_EN) can be programmed to transition from either the rising or falling edge of REF_CLK, and the timing is the same in either case. These options allows the use of non-compliant RMII PHYs.

Table 31. RMII transmit signal timing[1, 2]

Symbol		Characteristic	Value[3]		Unit
			Min	Max	
R5	CC	REF_CLK to TXD[1:0], TX_EN invalid	2	—	ns
R6	CC	REF_CLK to TXD[1:0], TX_EN valid	—	16	ns
R7	CC	REF_CLK pulse width high	35%	65%	REF_CLK period
R8	CC	REF_CLK pulse width low	35%	65%	REF_CLK period

1 RMII timing is valid only up to a maximum of 150 ^{o}C junction temperature.

2 All timing specifications are referenced for TTL or CMOS input levels for REF_CLK to the valid output levels, 0.8 V and 2.0 V.

3 Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

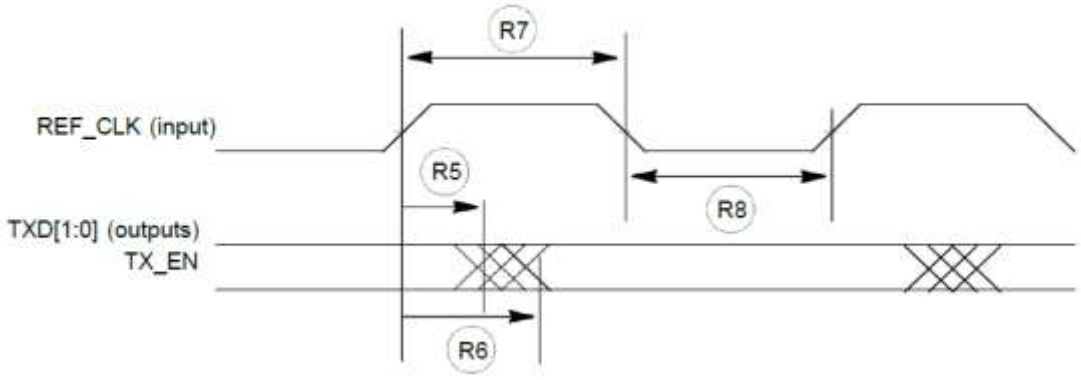


Figure 27. RMII transmit signal timing diagram

4 Package Information

4.1 416 TEPBGA (production) case drawing

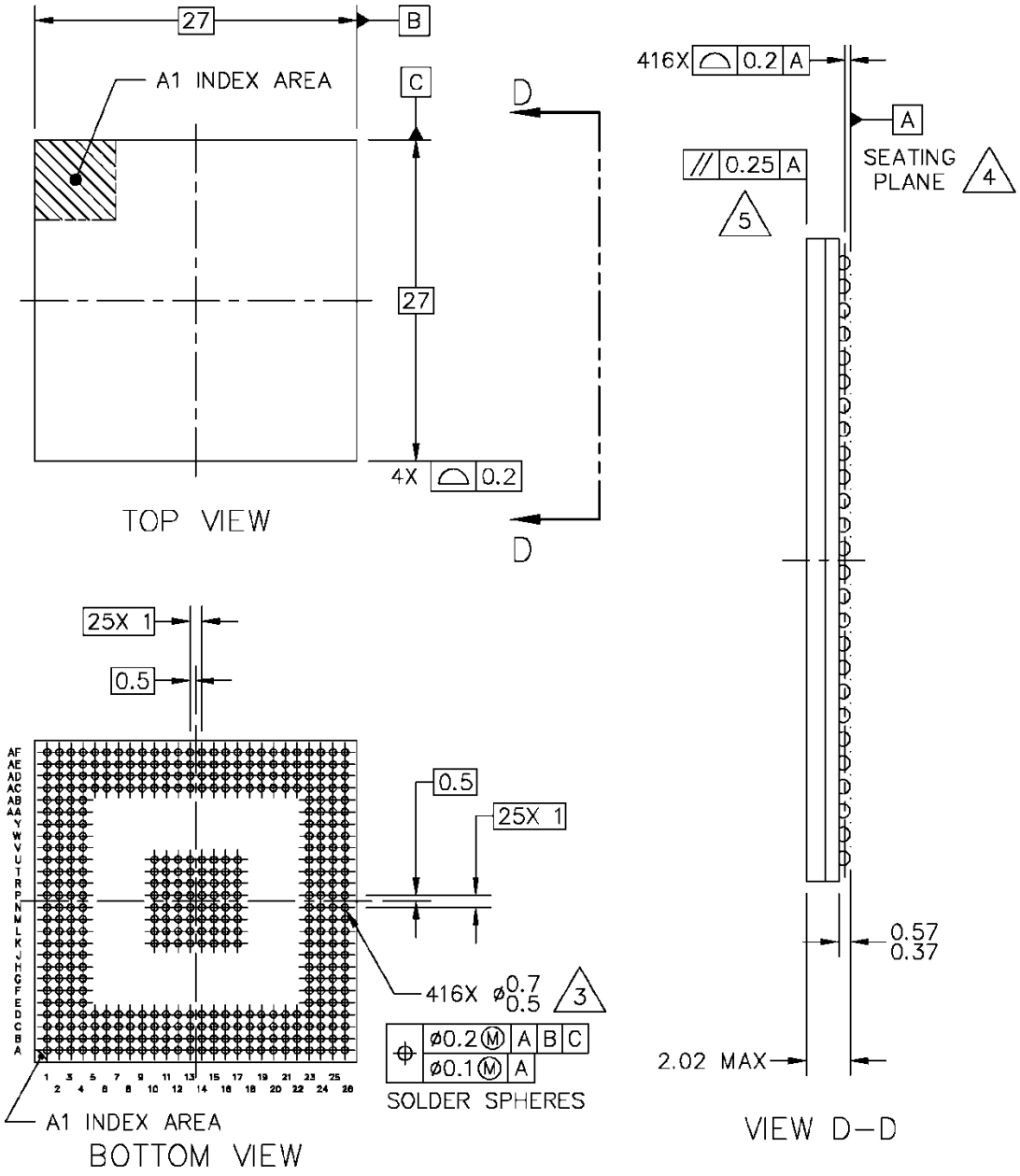


Figure 2. 416 TEPBGA (production) package mechanical drawing(Sheet 1 of 2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. DELETED IN REV O.

Figure 2. 416 TEPBGA (production) package mechanical drawing(Sheet 2 of 2)

4.2 216 HQFP (production) case drawing

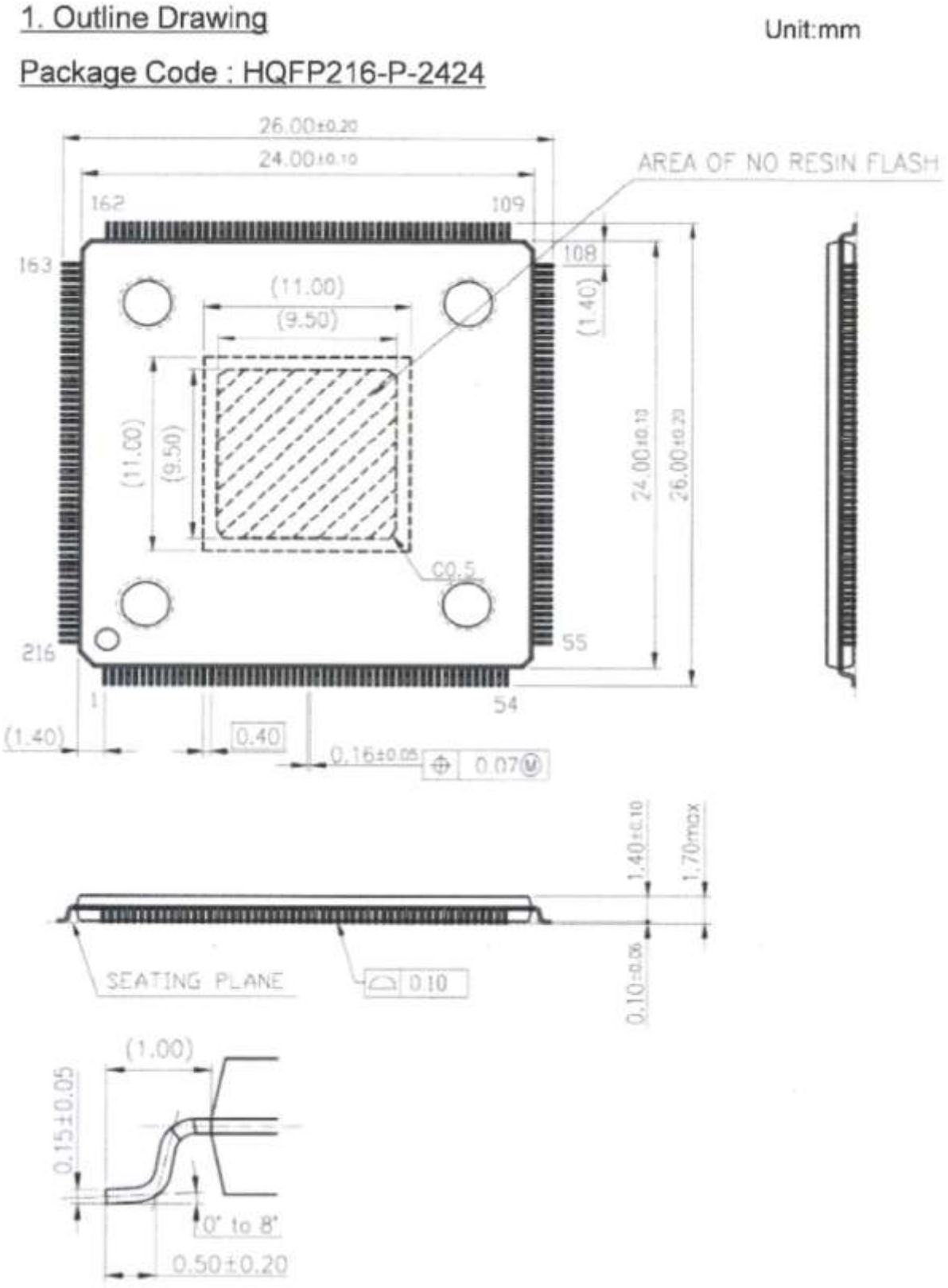


Figure 3. 216 HQFP (production) package mechanical drawing

5 Document revision history

Revision	Date	Description of changes
1.0	2023/6/5	Initial release
1.1	2023/6/9	Update CCFC3007PT pinmux and pinout.xlsx
1.2	2023/6/16	Update CCFC3007PT pinmux and pinout.xlsx
1.3	2023/7/27	Change name from CCFC3008PT200 to CCFC3007PT
1.4	2023/8/8	Modify CCFC3007PT family comparison Table Table 4 Device operating conditions Min Value modify