

Memory Controller Module

Summary

The Off-Chip Memory Controller allows various memory devices to connect to the NF46001 chip, through a shared 16-bit data bus and 21-bit address bus. Five memory segments are supported, each with its own chip-select. Memory segments can be programmed to support certain types of memory devices, such as Flash ROM, Mask ROM, DRAM, SRAM and SDRAM.

Features

The features of the Off-Chip Memory Controller include:

- Transparent operation
- Five memory segments (chip selects)
 - Three 4MB segments
 - Two 2MB segments
- 16-Bit data bus
 - Supports word, half word and byte transfers
- 21-bit address bus
 - Configurable 22nd bit for byte-size access
- Support static memories
 - Programmable access cycle time
 - Support Mask ROM, Flash ROM and SRAM
- Support dynamic memories
 - Programmable access cycle time
 - Programmable signal timing
 - Programmable refresh cycle time
 - Support DRAM and SDRAM
- Dual frequency
 - Normal 60MHz operation
 - Slower 30MHz operation

To obtain more information about the Memory Controller or other C*Core™ products, please contact the C*Core Technology Co., Ltd. by phone: 0512-68091377, email: support@china-core.com or web: <http://www.china-core.com>.
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