CCFC2003PT
Advance Information
Rev 2.3

HCMOS
Microcontroller Unit

IC Design Group
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Revision History

Release Number	Date	Author	Summary of Changes
0.4	2014.12.10	HWLIU	1) Add appendix A & B 2) Add 176pin package
0.6	2015.3.20	HWLIU	1) remove CLKOUT pin in 208/256 package type 2) assign PC[0:1] and PH[9:10] pin location at 208/256 package type
0.7	2015.4.20	HWLIU	1) assign PC[0:1] and PH[9:10] pin location at 208/256 package type 2) replace VDD33 with VDD5V at signal description and packge type 2) fixed appendix A electric characteristic at 2015.5.7
0.8	2015.6.19	HWLIU	1) fix some spelling error
0.9	2015.6.30	HWLIU	1) fix electrical characteristic
1.0	2015.7.17	HWLIU	1) fix format error 2) fix DSPI TFFF_RE description
1.1	2015.8.11	HWLIU	1) Add AC timing in appendix A
2.0	2015.9.20	HWLIU	1) fix QFP208 package signals
2.1	2016.8.3	HWLIU	1) add WKUP pins default state 2) add LQFP208 mechanical specifications
2.2	2017.3.17	HWLIU	1)remove PNP relative description and core voltage supply is fixed to external LDO circuit. 2)add power-up and power-down sequence
2.3	2018.12.11	HWLIU	1)add "13 different priorities can be configured to INTC_PSRx for one application" at INTC chapter 2)add "Interrupt request source must be level sense, and interrupt request source must keep active until cpu Acknowledg the interrupt" at INTC chapter

Section 1 Overview

Section 2 Memory Map

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Appendix A Preliminary Electrical Characteristic

Appendix B Mechanical Specifications

Section 1 Overview

1.1 Introduction

CCFC2003PT is a chip based on C2003 PowerPC processor. C2003 processor core is a single-issue, 4-pipeline, PowerPC processor which implements Power Architecture Book E programmer's model and VLE enhancements. CCFC2003PT is targeted to automotive-focused products.

CCFC2003PT uses one C2003 core and high-speed interconnect technolgy(AHB mixed matrix) to balance processor performance with I/O system throughout.

CCFC2003PT has an internal 128KBytes SRAM, an internal 1MB flash memory for data and 0.5MB flash memory for code, three flexCAN controller according to the CAN 2.0B protocol specification, two eMIOS controller to detect and measure the timing events, two LINFlex controller, two I2C controller, three DSPI controller, one ADC, ten program timer, one system timer, one software watchdog timer, an calibration external bus interface and the other miscellaneous periperals.

CCFC2003PT is designed for dynamic power management of core and peripherals. Software can controll the clock gating of peripherals.

1.2 Key Features

The following lists an overview of CCFC2003PT key feature set:

- Operation Parameters
  - Up to 80MHz operation frequency
  - –45 ˚C to 125 ˚C junction temperature operating range
- C2003 Cores
  - Single-issue, 4-pipeline PowerPC processor
  - 32-bit Power Architecture Book E programmer's model
  - Variable Length Encoding Enhancements
  - Separate instruction bus and load/store bus
  - Memory management unit with 16-entry TLB
  - Vectored interrupt support
  - Non-maskable interrupt(NMI) input for handling emergent external events

  - Scalar single precision FPU
- AHB Bus Controller
  - master ports
  - slave ports
  - 32-bit address, 64-bit data paths
  - Fully concurrent transfers between independent master and slave ports
  - Fixed priority scheme and fixed parking strategy
  - Force round_robin mode
- eFLASH
  - Total 1.5MBytes: 512KBytes for code storage and 1024KBytes for data storage
  - 128bits High read parallelism
  - SEC/DED
  - 64bits double word program
  - Sector erase
  - No support for read while write
  - Erase suspend
  - Software programmable program/erase/protection to avoid unwanted writings
  - Censored Mode against piracy
  - Shadow Sector Available for CFLASH
  - One-Time Programmable (OTP) area in Test Flash Block
  - (6)Boot sectors for CFLASH
- Internal SRAM
  - Total 128KBytes SRAM memory
  - Byte, halfword and word addressable
  - ECC (error correction code) protected with single-bit correction and double-bit detection
- BAM
  - Manages the serial download (FlexCAN or LINFlex protocols supported) including support for a serial password if censorship is enabled
  - Places the microcontroller into static mode if flash memory boot mode is selected and a valid BOOT_ID is not located in one of the boot sectors by the SSCM

  - System Configuration and Status
  - Memory sizes/status
  - Microcontroller Mode and Security Status
  - Search Code Flash for bootable sector
  - Determine boot vector
  - Device identification information
  - Debug Status Port enable and selection
  - Bus and peripheral abort enable/disable
- DSPI x 3
  - Full-duplex, three-wire synchronous transfers
  - Master and slave mode
  - Buffered transmit and receive operation using the TX and RX FIFOs, with depths of four entries
  - Visibility into TX and RX FIFOs for ease of debugging
  - FIFO bypass mode for low-latency updates to SPI queues
  - Programmable transfer attributes on a per-frame basis
  - Up to 6 peripheral chip selects, expandable to 64 with external demultiplexer
  - Deglitching support for up to 32 peripheral chip selects with external demultiplexer
  - 6 interrupt conditions:
  - Modified SPI transfer formats for communication with slower peripheral devices
  - Supports all functional modes from QSPI subblock of QSMCM
  - Continuous serial communications clock (SCK)
- ADC
  - 2 independent on-chip SAR ADCs
  - 8, 10, and 12-bit AD resolution
  - 500K Sample/s (ADC_CLK = 8 MHz) and 1M Sample/s (ADC_CLK = 16 MHz) for conversions
  - common mode conversion range (0–5V; 0–2.5V)
  - Differential conversions
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
  - Provides time stamp information when requested

  - Parallel interface to eQADC CFIFOs and RFIFOs
  - Supports both right-justified unsigned and signed formats for conversion results
  - Temperature sensor
  - Ability to measure directly VDD
  - 36 input channels available to the 2 on-chip ADCs
  - 4 pairs of differential analog input channels
  - Parallel Side Interface to communicate with decimation filter
  - Priority based CFIFOs
  - Supports six CFIFOs with fixed priority. The lower the CFIFO number, the higher its priority. When commands of distinct CFIFOs are bound for the same CBuffer, the higher priority CFIFO is always served first.
  - Immediate conversion command feature with conversion abort control
  - Streaming mode operation of CFIFO0 to execute some commands several times
  - Supports software and several hardware trigger modes to arm a particular CFIFO
  - Generates interrupt when command coherency is not achieved
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter
  - Supports controls to bypass the trigger digital filters
  - Additional internal trigger (not filtered) called Advance trigger that is used to enable the external trigger of queue0 and to control the loop behavior of CFIFO0
  - Supports 4 external 8-to-1 muxes which can expand the input channel number
- INTC
  - Supports 134 peripheral and 8 software-configurable interrupt request sources
  - Unique 9-bit vector per interrupt source
  - Each interrupt source can be programmed to one of 16 priorities
  - Preemption
  - Low latency - 3 clocks from receipt of interrupt request from peripheral to interrupt request to processor
- LINFlex x 2
  - Supports LIN protocol versions 1.3, 2.0, 2.1 and J2602
  - Master mode with autonomous message handling
  - Classic and enhanced checksum calculation and check

  - Single 8-byte buffer for transmission/reception
  - Extended frame mode for In-Application Programming (IAP) purposes
  - Wake-up event on dominant bit detection
  - True LIN field state machine
  - Advanced LIN error detection
  - Header, response and frame timeout
  - Slave mode1
  - Autonomous header handling
  - Autonomous transmit/receive data handling
  - LIN automatic resynchronization, allowing operation with 16 MHz fast internal RC oscillator as clock source
  - 16 identifier filters for autonomous message handling in Slave mode1
- SIUL x 1
  - Port funciton mutiplex
  - GPIO
  - External interrupts
  - System configuration
  - eQADC hardware triggers
- FlexCANx3
  - Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0-8 bytes data length
  - Programmable bit rate up to 1 Mbit/s
  - Content-related addressing
  - Flexible Message Buffers (up to 64) of zero to eight bytes data length
  - Each MB configurable as Rx or Tx, all supporting standard and extended messages
  - Individual Rx Mask Registers per Message Buffer
  - Includes either 1056 bytes (64 MBs) of SRAM used for MB storage
  - Includes either 256 bytes (64 MBs) of SRAM used for individual Rx Mask Registers
  - Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling

  - Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 8 extended, 16
  - standard or 32 partial (8 bits) IDs, with individual masking capability
  - Selectable backwards compatibility with previous FlexCAN version
  - Programmable clock source to the CAN Protocol Interface, either bus clock or crystal oscillator
  - Unused MB and Rx Mask Register space can be used as general purpose SRAM space
  - Listen-only mode capability
  - Programmable loop-back mode supporting self-test operation
  - Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
  - Time Stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
  - Independent of the transmission medium (an external transceiver is assumed)
  - Short latency time due to an arbitration scheme for high-priority messages
  - Low power mode
- IIC x2
  - Supports slave/master mode
  - Supports 7 bit addressing.
  - Supports Standard Mode, Fast Mode and High-Speed Mode
  - Software option to select between High-Speed mode and Standard/Fast mode
  - Compatibility with standard and fast-mode of I2C bus version 2.1 standard.
  - Multiple-master operation.
  - Software-programmable for one of 64 different serial clock frequencies.
  - Software-selectable acknowledge bit.
  - Interrupt-driven, byte-by-byte data transfer.
  - Arbitration-lost interrupt with automatic mode switching from master to slave.
  - Transfer completion and read configure interrupt.
  - Start and stop signal generation/detection.
  - Repeated START signal generation.

  - Acknowledge bit generation/detection.
  - Bus-busy detection.
  - Option slave address receiving enable when system clock stop mode
  - SCL or SDA line gpio function supported
- eMIOS x2
  - 50 channels with OPWMT
  - 6 channels with single action IC/OC
  - Both eMIOS blocks can be synchronized
  - One global prescaler
  - 32-bit data registers
  - 10 x 32-bit wide counter buses
    - Counter buses B, C, D, and E can be driven by Unified Channel 0, 8, 16, and 24, respectively
    - Counter bus A is driven by the Unified Channel #23
    - Several channels have their own time base, alternative to the counter buses
    - Shared timebases through the counter buses
    - Synchronization among timebases
  - Control and Status bits grouped in a single register
  - Shadow FLAG register
  - State of the UC can be frozen for debug purposes
    - Motor control capability
- CGM
  - Generates system and peripheral clocks
  - Selects and enables/disables the system clock supply from system clock sources according to MC_ME control
  - Contains a set of registers to control clock dividers for divided clock generation
  - Supports multiple clock sources and maps their address spaces to its memory map
  - Generates an output clock
  - Guarantees glitch-less clock transitions when changing the system clock selection
  - Supports 8-, 16- and 32-bit wide read/write accesses
- RGM
  - 'destructive' resets management

  - 'functional' resets management
  - signalling of reset events after each reset sequence (reset status flags)
  - conversion of reset events to SAFE mode or interrupt request events
  - short reset sequence configuration
  - bidirectional reset behavior configuration
  - selection of alternate boot via the backup SRAM on STANDBY mode exit
  - boot mode capture on RESET deassertion
- MC_ME
  - control of the available modes by the MC_ME register
  - definition of various device mode configurations by the ME_<mode>_MC registers
  - control of the actual device mode by the ME_MCTL register
  - capture of the current mode and various resource status within the contents of the ME_GS register
  - optional generation of various mode transition interrupts
  - status bits for each cause of invalid mode transitions
  - peripheral clock gating control based on the ME_RUN_PC0…7, ME_LP_PC0…7, and ME_PCTL0…143 registers
  - capture of current peripheral clock gated/enabled status
- CAN Sampler
  - Store 384 samples, equivalent to 48 CAN bit @ 8 samples/bit
  - Sample frequency from 500 kHz up to 16 MHz, equivalent at 8 samples/bit to CAN baud rates of 62.5 Kbps to 2 Mbps
  - User selectable CAN Rx sample port [CAN0RX-CAN5RX]
  - 16 MHz fast internal RC oscillator clock
  - 5-bit clock prescaler
  - Configurable trigger mode (immediate, next frame)
  - Flexible samples processing by software
  - Very low power consumption
- PIT
  - Support 10 channel with 32-bit width counter
  - Each timers can generate an individual interrupt request when timeout

  - Accessiable individual counter
  - Each channel can be controlled independently
  - Target value for each channel can be configured seperately
  - All interrupts are maskable
  - Independent timeout periods for each timer
- STM
  - One 32-bit up counter with 8-bit prescaler
  - Four 32-bit compare channels
  - Independent interrupt source for each channel
  - Counter can be stopped in debug mode
- SWT
  - 32-bit time-out register to set the time-out period
  - The unique SWT counter clock is the undivided slow internal RC oscillator 128 kHz (SIRC), no other clock source can be selected
  - Programmable selection of window mode or regular servicing
  - Programmable selection of reset or interrupt on an initial time-out
  - Master access protection
  - Hard and soft configuration lock bits
  - The SWT is started on exit of power-on phase (RGM phase 2) to monitor flash boot sequence phase. It is then reset during RGM phase3 and optionally enabled when platform reset is released depending on value of flash user option bit 31 (WATCHDOG_EN).
- ECSM
  - Program-visible information on the device configuration and revision
  - Registers for capturing information on memory errors due to error-correction codes
  - Registers to specify the generation of single- and double-bit memory data inversions for test purposes to check ECC protection
  - Configuration for additional SRAM WS for system frequency above 64 + 4% MHz
- SSCM
  - System Configuration and Status
    - Memory sizes/status
    - Microcontroller Mode and Security Status (including censorship and serial boot information)

    - Search Code Flash for bootable sector
    - Determine boot vector
  - Device identification information (MCU ID Registers)
  - Debug Status Port enable and selection
  - Bus and peripheral abort enable/disable
- WKUP
  - Non-maskable interrupt support with
    - 1 NMI source with bypassable glitch filter
    - Independent interrupt destination: non-maskable interrupt, critical interrupt, or machine check request
    - Edge detection
  - External wakeup/interrupt support with
    - 3 system interrupt vectors for up to 18 interrupt sources
    - Analog glitch filter per each wakeup line
    - Independent interrupt mask
    - Edge detection
    - Configurable system wakeup triggering from all interrupt sources
    - Configurable pullup
- CMU
  - FIRC, SIRC, SXOSC oscillator frequency measurement using FXOSC as reference clock
  - External oscillator clock monitoring with respect to FIRC_clk/n clock
  - FMPLL clock frequency monitoring for a high and low frequency range with FIRC as reference clock
  - Event generation for various failures detected inside monitoring unit
- DMA
  - Support for 32 channel.
  - Connections to the AMBA-AHB crossbar switch for bus mastering the data movement, slave bus for programming the module
    - Support for 64-bit AMBA-AHB datapath widths
  - 32-byte transfer control descriptor per channel stored in local memory
  - 32 bytes of data registers, used as temporary storage to support burst transfers.
  - All data movement via dual-address transfers: read from source, write to destination

    - Programmable source, destination addresses, transfer size, plus support for enhanced addressing modes
  - Transfer control descriptor organized to support two-deep, nested transfer operations
    - An inner data transfer loop defined by a “minor” byte transfer count
    - An outer data transfer loop defined by a “major” iteration count
  - Channel service request via one of three methods:
    - Explicit software initiation
    - Initiation via a channel-to-channel linking mechanism for continuous transfers Independent channel linking at end of minor loop and/or major loop
    - Peripheral-paced hardware requests (one per channel)
    - For all three methods, one service request per execution of the minor loop is required.
  - Support for fixed-priority and round-robin channel arbitration
  - Channel completion reported via optional interrupt requests
    - One interrupt per channel, optionally asserted at completion of major iteration count
    - Error terminations are optionally enabled per channel, and logically summed together to form a small number of error interrupt outputs
    - Support for scatter/gather DMA processing
- EBI
  - Reduced system complexity — No external glue logic required for typical system if chip selects are used.
  - Two asynchronous active-low chip selects can be independently programmed with various features.
  - Support 128Mbyte block sizes for per chip select.
  - Support for 8-bit, 16-bit, and 32-bit devices for per chip select.
  - Programmable write protection — Each chip select address range can be designated for read access only.
  - Programmable access protection — Each chip select address range can be designated for supervisor access only.
  - Write-enable eb[3:0] selection — The enable byte pins can be configured as byte enables(assert on both external read and write accesses) or write enables(only assert on external write access)
  - Bus cycle termination — The chip select logic to terminate the bus cycle.
  - Programmable wait states — To interface with various devices, up to seven wait states can be Programmed before the access is terminated.

– Programmable extra wait state for write accesses — One wait state can be added to write accesses to allow writing to memories that require additional data setup time.

1.3 Block Diagram

Figure 1-1 is a block diagram of the system view.

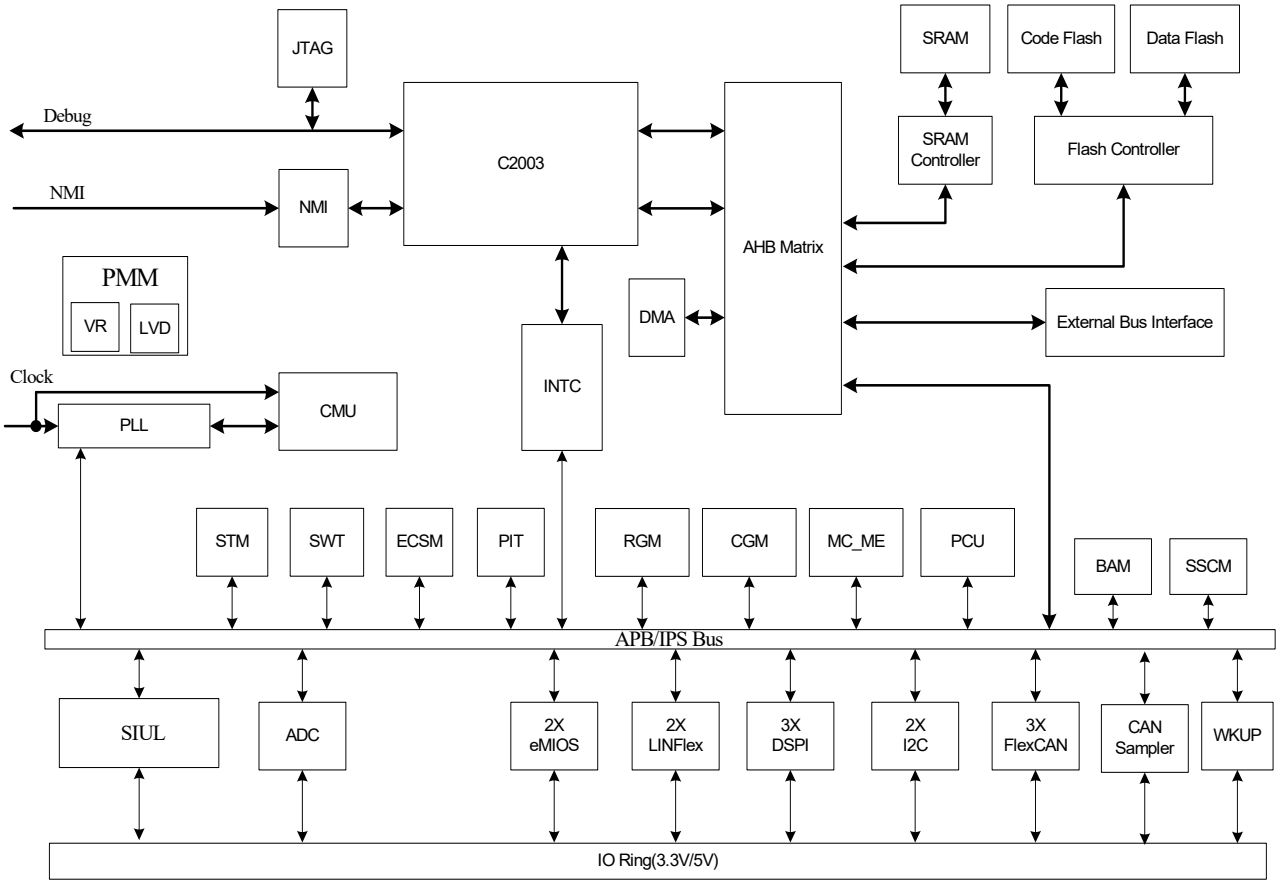


Figure 1-1 Block Diagram

Overview

Section 2 Memory Map

This chapter presents the memory map for this device.

2.1 Introduction

All addresses in the device, including those that are reserved, are identified in the tables. The addresses represent the physical addresses assigned to each IP block. Logical addresses are translated by the Memory Management Unit (MMU) into physical addresses.

Under software control of the MMU, the logical addresses allocated to IP blocks may be changed on aminimum of a 4 KB boundary.

2.2 Address Map

Table 2-1 Address Map

Module	Address Range
Flash Bank0, Array0	0x0000_0000 ~ 0x0007_FFFF
Flash Bank1, Array1	0x0008_0000 ~ 0x000F_FFFF
Flash Bank1, Array2	0x0010_0000 ~ 0x0017_FFFF
Flash Bank1, Array2 Test Sector	0x00B7_FB00 ~ 0x00B7_FEFF
Flash Bank1, Array1 Test Sector	0x00BB_FB00 ~ 0x00BB_FEFF
Flash Bank0, Array0 Test Sector	0x00BF_FB00 ~ 0x00BF_FEFF
Reserved	0x00C0_0000 ~ 0x00FF_BFFF
Flash Shadow Block	0x00FF_C000 ~ 0x00FF_FFFF
Flash Emulation Mapping	0x0100_0000 ~ 0x1FFF_FFFF
Reserved for External Bus Interface	0x3000_0000 ~ 0x3FFF_FFFF
SRAM	0x4000_0000 ~ 0x4001_FFFF
Reserved	0x4000_C000 ~ 0xC3F8_3FFF
CEBI	0xC3F8_4000 ~ 0xC3F8_7FFF
Flash Bank0, Array0 Register	0xC3F8_8000 ~ 0xC3F8_BFFF
SIUL	0xC3F9_0000 ~ 0xC3F9_3FFF
WKUP	0xC3F9_4000 ~ 0xC3F9_7FFF
Reserved	0xC3F9_8000 ~ 0xC3F9_FFFF
eMIOS_0	0xC3FA_0000 ~ 0xC3FA_3FFF
eMIOS_1	0xC3FA_4000 ~ 0xC3FA_7FFF
DSPI_0	0xC3FA_8000 ~ 0xC3FA_BFFF

Table 2-1 Address Map

Module	Address Range
DSPI_1	0xC3FA_C000 ~ 0xC3FA_FFFF
Flash Bank1, Array1 Register	0xC3FB_0000 ~ 0xC3FB_3FFF
Flash Bank1, Array2 Register	0xC3FB_4000 ~ 0xC3FB_7FFF
DSPI_2	0xC3FB_8000 ~ 0xC3FB_BFFF
SSCM	0xC3FD_8000 ~ 0xC3FD_BFFF
MC_ME	0xC3FD_C000 ~ 0xC3FD_FFFF
Clock source	0xC3FE_0000 ~ 0xC3FE_003F
MC_CMU	0xC3FE_0100 ~ 0xC3FE_036F
MC_CGM	0xC3FE_0370 ~ 0xC3FE_03FF
MC_RGM	0xC3FE_4000 ~ 0xC3FE_7FFF
MC_PCU	0xC3FE_8000 ~ 0xC3FE_BFFF
Reserved	0xC3FE_C000 ~ 0xC3FE_FFFF
PIT	0xC3FF_0000 ~ 0xC3FF_3FFF
Reserved	0xC3FF_4000 ~ 0xFFDF_FFFF
ADC	0xFFE0_0000 ~ 0xFFE0_3FFF
Reserved	0xFFE0_4000 ~ 0xFFE2_FFFF
I2C0	0xFFE3_0000 ~ 0xFFE3_3FFF
I2C1	0xFFE3_4000 ~ 0xFFE3_7FFF
Reserved	0xFFE3_8000 ~ 0xFFE3_FFFF
LINFlex_0	0xFFE4_0000 ~ 0xFFE4_3FFF
LINFlex_1	0xFFE4_4000 ~ 0xFFE4_7FFF
Reserved	0xFFE4_8000 ~ 0xFFE4_BFFF
Reserved	0xFFE4_C000 ~ 0xFFE4_FFFF
Reserved	0xFFE5_0000 ~ 0xFFE6_3FFF
CTU	0xFFE6_4000 ~ 0xFFE6_7FFF
Reserved	0xFFE6_8000 ~ 0xFFE6_FFFF
CAN sampler	0xFFE7_0000 ~ 0xFFE7_3FFF
Reserved	0xFFE7_4000 ~ 0xFFE7_FFFF
Mirrored range 0x3F800000-0xC3FFFFFF	0xFFE8_0000 ~ 0xFFEF_FFFF
Reserved	0xFFF0_0000 ~ 0xFFF0_FFFF
Reserved	0xFFF1_0000 ~ 0xFFF1_3FFF
Reserved	0xFFF1_4000 ~ 0xFFF3_7FFF
SWT	0xFFF3_8000 ~ 0xFFF3_BFFF
STM	0xFFF3_C000 ~ 0xFFF3_FFFF
ECSM	0xFFF4_0000 ~ 0xFFF4_3FFF
DMA	0xFFF4_4000 ~ 0xFFF4_7FFF
INTC	0xFFF4_8000 ~ 0xFFF4_BFFF

Table 2-1 Address Map

Module	Address Range
Reserved	0xFFF4_C000 ~ 0xFFF8_BFFF
Decimation Filter	0xFFF8_C000 ~ 0xFFF8_FFFF
Reserved	0xFFF9_0000 ~ 0xFFFB_FFFF
FlexCAN_0	0xFFFC_0000 ~ 0xFFFC_3FFF
FlexCAN_1	0xFFFC_4000 ~ 0xFFFC_7FFF
FlexCAN_2	0xFFFC_8000 ~ 0xFFFC_BFFF
Reserved	0xFFFC_C000 ~ 0xFFFC_FFFF
Reserved	0xFFFD_0000 ~ 0xFFFD_3FFF
Reserved	0xFFFD_4000 ~ 0xFFFD_7FFF
Reserved	0xFFFD_8000 ~ 0xFFFF_BFFF
BAM	0xFFFF_C000 ~ 0xFFFF_FFFF

Memory Map

Section 3 Signal description

3.1 Introduction

The following sections provide signal descriptions and related information about the functionality and configuration.

3.2 Package pinouts

The LQFP pinouts are provided in the following figures.

For more information on pin multiplexing on this device, see **Table 3-1** through **Table 3-3**.

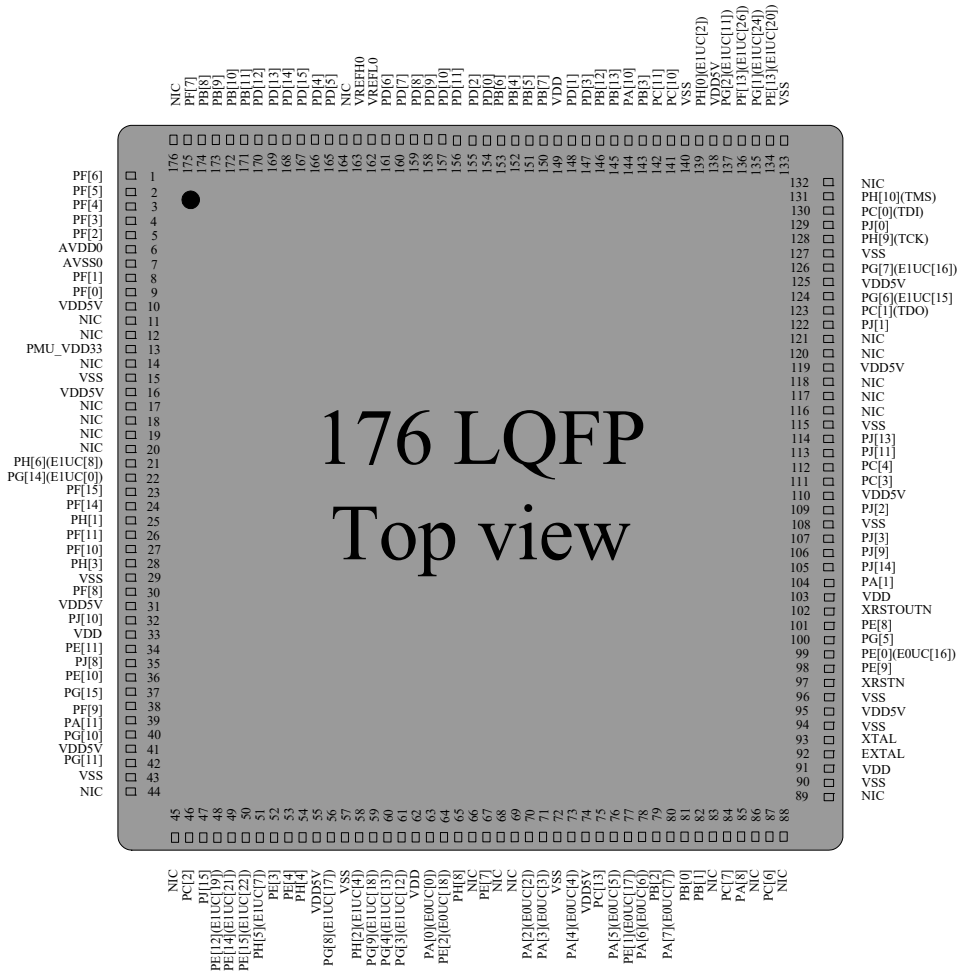


Figure 3-1 ccfc2003pt LQFQ 176-pin configuration

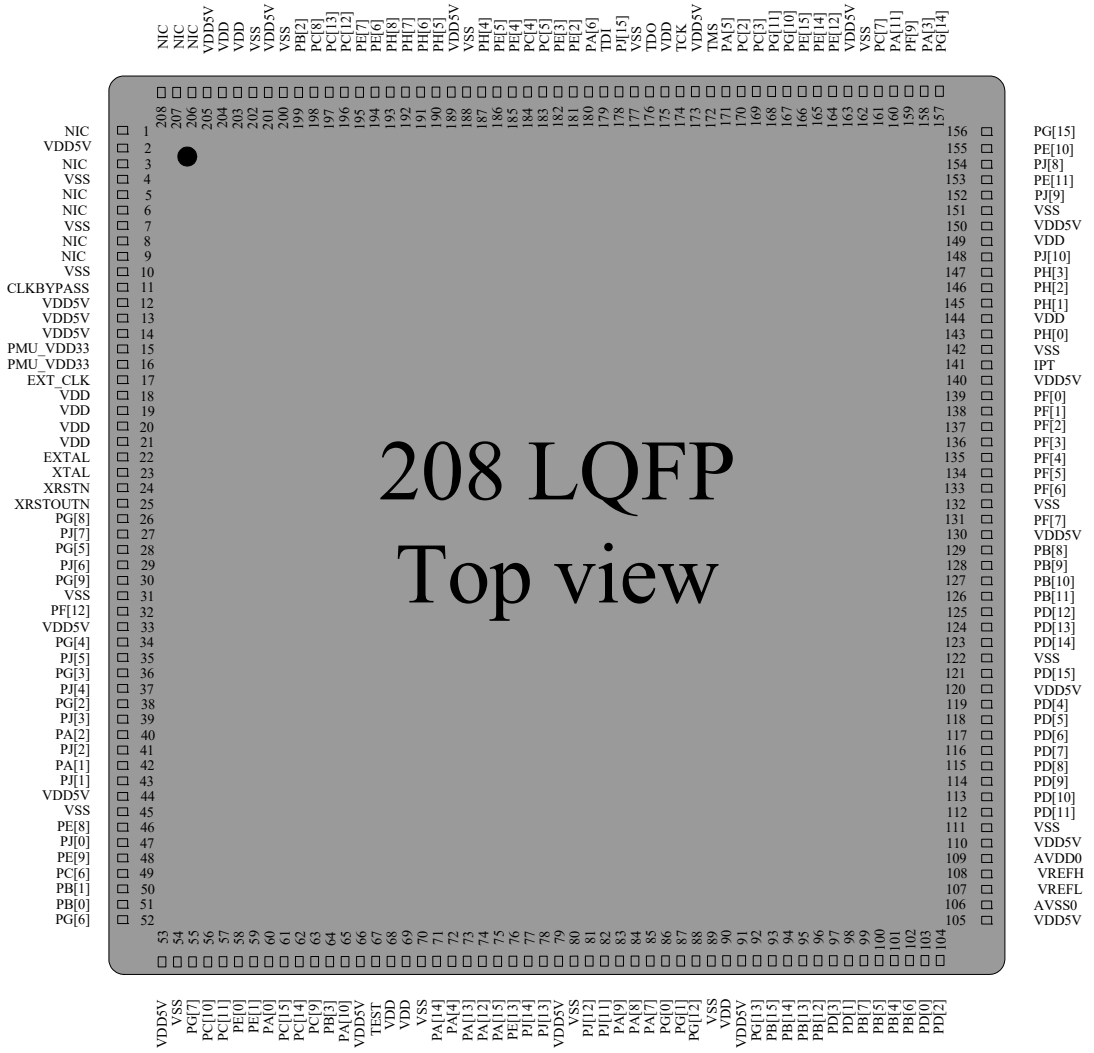
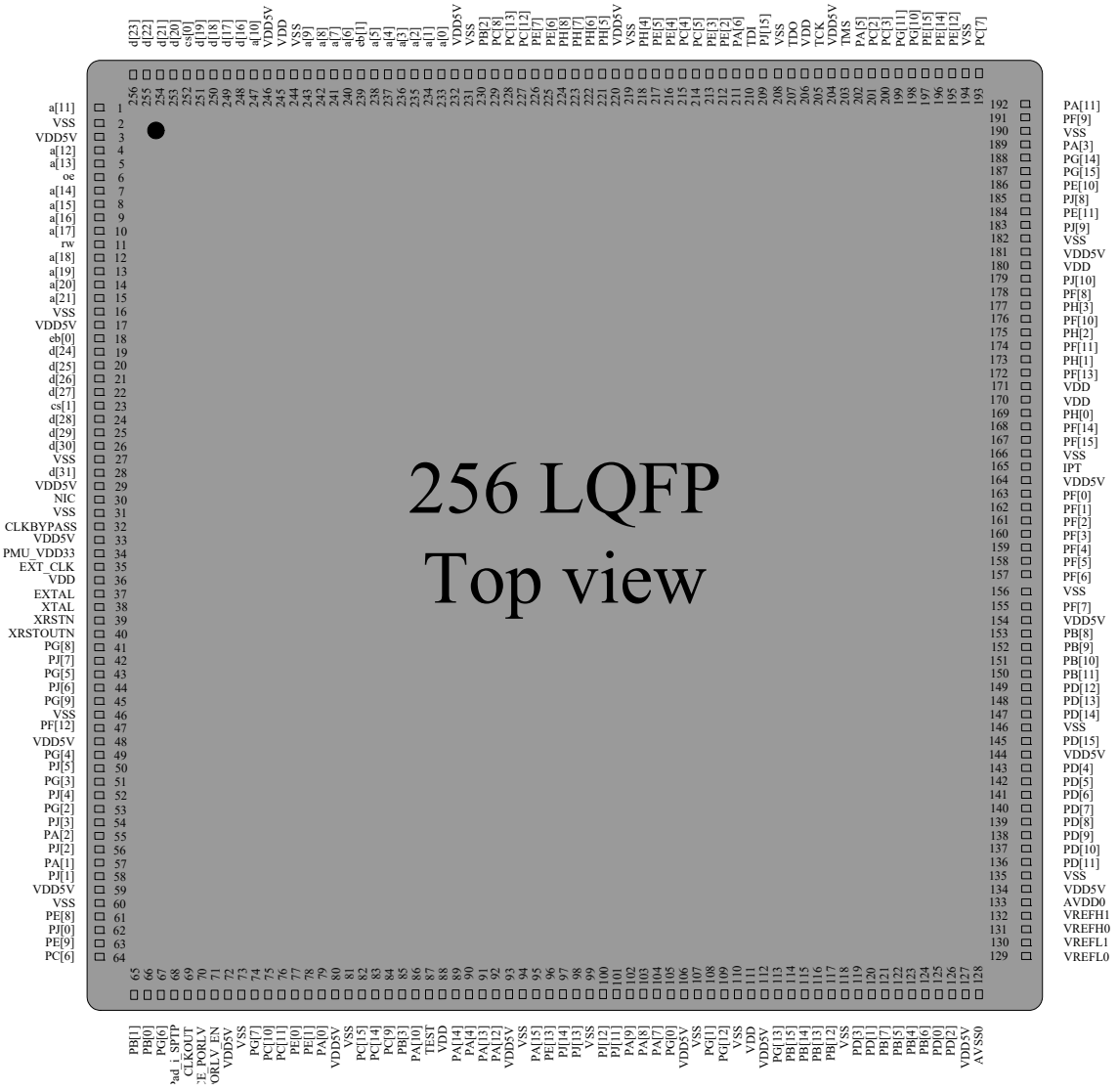


Figure 3-2 ccfc2003pt LQFP 208-pin configuration



Availability of port pin alternate functions depends on product selection.

Figure 3-3 LQFP 256-pin configuration (top view)

3.3 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-on phase, all pads are forced to tristate.

After power-on phase, all pads are forced to tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS[0]) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS and TDI) are pull-up whilst TDO remains tristate.
- Precise ADC pads (PB[7:4] and PD[11:0]) are left tristate (no output buffer available).
- Main oscillator pads (EXTAL, XTAL) are tristate.

3.4 System pins

The system pins are listed in **Table 3-1**.

Table 3-1 system pin descriptions

System pin	Function	I/O direction	RESET config.	Pin number		
				176 LQFP	208 LQFP	256 LQFP
XRSTOUTN	Internal reset indicator			102	25	40
XRSTN	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	Input, weak pull-up only after PHASE	97	24	39
EXTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.	I	Tristate	92	22	37
XTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	O	Tristate	93	23	38
EXT_CLK	External clock input if oscillator is used in bypass mode.	I	Input, weak pull-down	-	17	35

Table 3-1 system pin descriptions

CLKBYPASS	Clock bypass mode control and high active	I	Input, weak pull-down	-	11	32
FORCE_PORLV	Externl por input and low active	I	Input, weak pull-up	-	-	70
PORLV_EN	Internal POR circuit enable control and high active	I	Input, weak pull-up	-	-	71
PAD_I_SPTP	Main power supply voltage indicator and high stands for 5V power supply and low dor 3.3V power supply	I	Input, weak pull-up	-	-	68
IPT	Internal analog ip test mode and high active	I	Input, weak pull-down	-	141	165
TEST	SCAN and Internal analog ip test mode control and high active	I	Input, weak pull-down	-	67	87

3.5 Power pins

The power pins are listed in **Table 3-2**.

Table 3-2 power pin descriptions

System pin	Function	I/O direction	RESET config.	Pin number		
				176 LQFP	208 LQFP	256 LQFP
VDD	1.5V power supply	POWER	-	33,62,91,103,149	18,19,20,21,68,69,90,144,149,175,203,204	36,88,111,170,171,180,206,245

Table 3-2 power pin descriptions

VDD5V	Main power supply	POWER	-	10,16,31,41,55,74,95,110,119,125,138	2,205,163,53,110,173,120,66,130,189,12,13,14,79,,140,201,91,133,150,44,105	3,17,29,246,72,134,204,80,144,154,220,93,33,164,232,106,112,48,181,59,127
PMU_VDD33	Internal 3.3V LDO output	POWER	-	13	15,16	34

3.6 Functional ports

The functional port pins are listed in **Table 3-3**.

Table 3-3 Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	RESET configuration	Pin number		
							176 LQFP	208 LQFP	256 LQFP[3]
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT — WKUP[19][4]	SIUL eMIOS_0 CGL — WKPU	I/O I/O O — I	Tristate	63	60	79

Table 3-3 Functional port pin descriptions

PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — —	GPIO[1] E0UC[1] — — NMI[5] WKUP[2][4]	SIUL eMIOS_0 — — WKPU WKPU	I/O I/O — — I I	Tristate	104	42	57
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — — WKUP[3][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	Tristate	70	40	55
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 —	GPIO[3] E0UC[3] — — EIRQ[0]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	Tristate	71	158	189
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — — WKUP[9][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	Tristate	73	72	90
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	Tristate	76	171	202
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — — EIRQ[1]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	Tristate	78	180	211
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 —	GPIO[7] E0UC[7] — — EIRQ[2]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	Tristate	80	85	104
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A	GPIO[8] E0UC[8] — — EIRQ[3] ABS[0]	SIUL eMIOS_0 — — SIUL BAM	I/O I/O — — I I	Input, weak pull-up	85	84	103
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A	GPIO[9] E0UC[9] — — FAB	SIUL eMIOS_0 — — BAM	I/O I/O — — I	Pull-down	—	83	102

Table 3-3 Functional port pin descriptions

PA[10]	PCR[10]	AF0 AF1 AF2 AF3	GPIO[10] E0UC[10] SDA0 —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	Tristate	144	65	86
PA[11]	PCR[11]	AF0 AF1 AF2 AF3	GPIO[11] E0UC[11] SCL0 —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	Tristate	39	160	192
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 —	GPIO[12] — — — SIN_0	SIUL — — — DSPI0	I/O — — — I	Tristate	—	74	92
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 — —	SIUL DSPI_0 — —	I/O O — —	Tristate	—	73	91
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 — EIRQ[4]	SIUL DSPI_0 DSPI_0 — SIUL	I/O I/O I/O — I	Tristate	—	71	89
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 — WKUP[10][4]	SIUL DSPI_0 DSPI_0 — WKPU	I/O I/O I/O — I	Tristate	—	75	95
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX — —	SIUL FlexCAN_0 — —	I/O O — —	Tristate	81	51	66
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — —	GPIO[17] — — — WKUP[4][4] CAN0RX	SIUL — — — WKPU FlexCAN_0	I/O — — — I I	Tristate	82	50	65
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA0 —	SIUL LINFlex_0 I2C_0 —	I/O O I/O —	Tristate	79	199	230

Table 3-3 Functional port pin descriptions

PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] — SCL0 — WKUP[11][4] LIN0RX	SIUL — I2C_0 — WKPU LINFlex_0	I/O — I/O — I I	Tristate	143	64	85
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 —	GPIO[20] — — — AN0	SIUL — — — ADC	I/O — — — I	Tristate	152	101	123
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 —	GPIO[21] — — — AN1	SIUL — — — ADC	I/O — — — I	Tristate	151	100	122
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 —	GPIO[22] — — — AN2	SIUL — — — ADC	I/O — — — I	Tristate	153	102	124
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — AN3	SIUL — — — ADC	I/O — — — I	Tristate	150	99	121
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 —	GPIO[24] — — — AN16	SIUL — — — ADC	I/O — — — I	Tristate	174	129	153
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — AN17	SIUL — — — ADC	I/O — — — I	Tristate	173	128	152
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — AN18 WKUP[8][4]	SIUL — — — ADC WKPU	I/O — — — I I	Tristate	172	127	151

Table 3-3 Functional port pin descriptions

PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 AN19	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	Tristate	171	126	150
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 AN32	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	Tristate	146	96	117
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 AN33	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	Tristate	145	95	116
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 AN34	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	Tristate	—	94	115
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 AN35	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	Tristate	—	93	114
PC[0][7]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	Input, weak pull-up	130	179	210
PC[1][7]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	Tristate	123	176	207
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 — — EIRQ[5]	SIUL DSPI_1 — — SIUL	I/O I/O O — I	Tristate	46	170	201
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] — CAN1RX — EIRQ[6]	SIUL DSPI_1 ADC — FlexCAN_1 — SIUL	I/O I/O O — I I I	Tristate	111	169	200

Table 3-3 Functional port pin descriptions

PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — —	GPIO[36] — — — SIN_1 —	SIUL — — — DSPI_1 —	I/O — — — I I	Tristate	112	184	215
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 — — EIRQ[7]	SIUL DSPI1 — — SIUL	I/O O O — I	Tristate	—	183	214
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX — —	SIUL LINFlex_1 — —	I/O O — —	Tristate	87	49	64
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — — — LIN1RX WKUP[12][4]	SIUL — — — LINFlex_1 WKPU	I/O — — — I I	Tristate	84	161	193
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] — — —	SIUL — — —	I/O — — —	Tristate	—	198	229
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — — — — WKUP[13][4]	SIUL — — — — WKPU	I/O — — — — I	Tristate	—	63	84
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX — MA[1]	SIUL FlexCAN_1 — ADC	I/O O O O	Tristate	141	56	75
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — — CAN1RX — WKUP[5][4]	SIUL — — — FlexCAN_1 — WKPU	I/O — — — I I I	Tristate	142	57	76

Table 3-3 Functional port pin descriptions

PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — SIN_2	SIUL eMIOS_0 — — DSPI_2	I/O I/O — — I	Tristate	—	196	227
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	Tristate	75	197	228
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	Tristate	—	62	83
PC[15]	PCR[47]	AF0 AF1 AF2 AF3	GPIO[47] E0UC[15] CS0_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O I/O —	Tristate	—	61	82
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 —	GPIO[48] — — — AN4	SIUL — — — ADC	I — — — I	Tristate	154	103	125
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 —	GPIO[49] — — — AN5	SIUL — — — ADC	I — — — I	Tristate	148	98	120
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 —	GPIO[50] — — — AN6	SIUL — — — ADC	I — — — I	Tristate	155	104	126
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 —	GPIO[51] — — — AN7	SIUL — — — ADC	I — — — I	Tristate	147	97	119
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 —	GPIO[52] — — — AN8	SIUL — — — ADC	I — — — I	Tristate	166	119	143

Table 3-3 Functional port pin descriptions

PD[5]	PCR[53]	AF0 AF1 AF2 AF3 —	GPIO[53] — — — AN9	SIUL — — — ADC	I — — — I	Tristate	165	118	142
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 —	GPIO[54] — — — AN10	SIUL — — — ADC	I — — — I	Tristate	161	117	141
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 —	GPIO[55] — — — AN11	SIUL — — — ADC	I — — — I	Tristate	160	116	140
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 —	GPIO[56] — — — AN12	SIUL — — — ADC	I — — — I	Tristate	159	115	139
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 —	GPIO[57] — — — AN13	SIUL — — — ADC	I — — — I	Tristate	158	114	138
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 —	GPIO[58] — — — AN14	SIUL — — — ADC	I — — — I	Tristate	157	113	137
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 —	GPIO[59] — — — AN15	SIUL — — — ADC	I — — — I	Tristate	156	112	136
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — AN20	SIUL DSPI_0 eMIOS_0 — ADC	I/O O I/O — I	Tristate	170	125	149
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — AN21	SIUL DSPI_1 eMIOS_0 — ADC	I/O I/O I/O — I	Tristate	169	124	148

Table 3-3 Functional port pin descriptions

PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — AN22	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	Tristate	168	123	147
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — AN23	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	Tristate	167	121	145
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] — — — WKUP[6][4]	SIUL eMIOS_0 — — — WKPU	I/O I/O — — I I	Tristate	99	58	77
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] — —	SIUL eMIOS_0 — —	I/O I/O O —	Tristate	77	59	78
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 —	GPIO[66] E0UC[18] — — SIN_1	SIUL eMIOS_0 — — DSPI_1	I/O I/O — — I	Tristate	64	181	212
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS_0 DSPI_1 —	I/O I/O O —	Tristate	52	182	213
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 — EIRQ[9]	SIUL eMIOS_0 DSPI_1 — SIUL	I/O I/O I/O — I	Tristate	53	185	216
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC	I/O I/O I/O O	Tristate	—	186	217
PE[6]	PCR[70]	AF0 AF1 AF2 AF3	GPIO[70] E0UC[22] CS3_0 MA[1]	SIUL eMIOS_0 DSPI_0 ADC	I/O I/O O O	Tristate	—	194	225

Table 3-3 Functional port pin descriptions

PE[7]	PCR[71]	AF0 AF1 AF2 AF3	GPIO[71] E0UC[23] CS2_0 MA[0]	SIUL eMIOS_0 DSPI_0 ADC	I/O I/O O O	Tristate	67	195	226
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX[12] E0UC[22] —	SIUL FlexCAN_2 eMIOS_0 —	I/O O I/O O	Tristate	101	46	61
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKUP[7][4] CAN2RX —	SIUL — eMIOS_0 — WKPU FlexCAN_2 —	I/O — I/O — I I I	Tristate	98	48	63
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] — CS3_1 — EIRQ[10]	SIUL — DSPI_1 — SIUL	I/O — O — I	Tristate	36	155	186
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] — CS4_1 — — WKUP[14][4]	SIUL — DSPI_1 — — WKPU	I/O — O — — I	Tristate	34	153	184
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — —	GPIO[76] — E1UC[19] — SIN_2 EIRQ[11]	SIUL — eMIOS_1 — DSPI_2 SIUL	I/O — I/O — I I	Tristate	48	164	195
PE[13]	PCR[77]	AF0 AF1 AF2 AF3	GPIO[77] SOUT2 E1UC[20] —	SIUL DSPI_2 eMIOS_1 —	I/O O I/O —	Tristate	134	76	96
PE[14]	PCR[78]	AF0 AF1 AF2 AF3 —	GPIO[78] SCK_2 E1UC[21] — EIRQ[12]	SIUL DSPI_2 eMIOS_1 — SIUL	I/O I/O I/O — I	Tristate	49	165	196

Table 3-3 Functional port pin descriptions

PE[15]	PCR[79]	AF0 AF1 AF2 AF3	GPIO[79] CS0_2 E1UC[22] —	SIUL DSPI_2 eMIOS_1 —	I/O I/O I/O —	Tristate	50	166	197
PF[0]	PCR[80]	AF0 AF1 AF2 AF3 —	GPIO[80] E0UC[10] CS3_1 — AN24	SIUL eMIOS_0 DSPI_1 — ADC	I/O I/O O — I	Tristate	9	139	163
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — AN25	SIUL eMIOS_0 DSPI_1 — I	I/O I/O O — I	Tristate	8	138	162
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — AN26	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O I/O — I	Tristate	5	137	161
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — AN27	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	Tristate	4	136	160
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — AN28	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	Tristate	3	135	159
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — AN29	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	Tristate	2	134	158
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] — — AN30	SIUL eMIOS_0 — — ADC	I/O I/O — — I	Tristate	1	133	157
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — — — AN31	SIUL — — — ADC	I/O — — — I	Tristate	175	131	155

Table 3-3 Functional port pin descriptions

PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] — CS4_0 CAN2TX	SIUL — DSPI_0 FlexCAN_2	I/O O O O	Tristate	30	—	178
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — —	GPIO[89] — CS5_0 — CAN2RX —	SIUL — DSPI_0 — FlexCAN_2 —	I/O — O — I I	Tristate	38	159	191
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] — — —	SIUL — — —	I/O — — —	Tristate	27	—	176
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 —	GPIO[91] — — — WKUP[15][4]	SIUL — — — WKPU	I/O — — — I	Tristate	26	—	174
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] — —	SIUL eMIOS_1 — —	I/O I/O — —	Tristate	—	32	47
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 —	GPIO[93] E1UC[26] — — WKUP[16][4]	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	Tristate	136	—	172
PF[14]	PCR[94]	AF0 AF1 AF2 AF3	GPIO[94] — E1UC[27] CAN1TX	SIUL — eMIOS_1 FlexCAN_1	I/O O I/O O	Tristate	24	—	168
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — —	GPIO[95] — — — CAN1R — EIRQ[13]	SIUL — — — FlexCAN_1 — SIUL	I/O — — — — I I I	Tristate	23	—	167

Table 3-3 Functional port pin descriptions

PG[0]	PCR[96]	AF0 AF1 AF2 AF3	GPIO[96] — E1UC[23] —	SIUL — eMIOS_1 —	I/O O I/O —	Tristate	—	86	105
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — —	GPIO[97] — E1UC[24] — — EIRQ[14]	SIUL — eMIOS_1 — — SIUL	I/O — I/O — I I	Tristate	135	87	108
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] — —	SIUL eMIOS_1 — —	I/O I/O — —	Tristate	137	38	53
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] — — WKUP[17][4]	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	Tristate	61	36	51
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] — —	SIUL eMIOS_1 — —	I/O I/O — —	Tristate	60	34	49
PG[5]	PCR[101]	AF0 AF1 AF2 AF3 —	GPIO[101] E1UC[14] — — WKUP[18][4]	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	Tristate	100	28	43
PG[6]	PCR[102]	AF0 AF1 AF2 AF3	GPIO[102] E1UC[15] — —	SIUL eMIOS_1 — —	I/O I/O — —	Tristate	124	52	67
PG[7]	PCR[103]	AF0 AF1 AF2 AF3	GPIO[103] E1UC[16] — —	SIUL eMIOS_1 — —	I/O I/O — —	Tristate	126	55	74
PG[8]	PCR[104]	AF0 AF1 AF2 AF3 —	GPIO[104] E1UC[17] — CS0_2 EIRQ[15]	SIUL eMIOS_1 — DSPI_2 SIUL	I/O I/O — I/O I	Tristate	56	26	41

Table 3-3 Functional port pin descriptions

PG[9]	PCR[105]	AF0 AF1 AF2 AF3	GPIO[105] E1UC[18] — SCK_2	SIUL eMIOS_1 — DSPI_2	I/O I/O — I/O	Tristate	59	30	45
PG[10]	PCR[106]	AF0 AF1 AF2 AF3	GPIO[106] E0UC[24] — —	SIUL eMIOS_0 — —	I/O I/O — —	Tristate	40	167	198
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] — —	SIUL eMIOS_0 — —	I/O I/O — —	Tristate	42	168	199
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] — —	SIUL eMIOS_0 — —	I/O I/O — —	Tristate	—	88	109
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] — —	SIUL eMIOS_0 — —	I/O I/O — —	Tristate	—	92	113
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] — —	SIUL eMIOS_1 — —	I/O I/O — —	Tristate	22	157	188
PG[15]	PCR[111]	AF0 AF1 AF2 AF3	GPIO[111] E1UC[1] — —	SIUL eMIOS_1 — —	I/O I/O — —	Tristate	37	156	187
PH[0]	PCR[112]	AF0 AF1 AF2 AF3 —	GPIO[112] E1UC[2] — — SIN1	SIUL eMIOS_1 — — DSPI_1	I/O I/O — — I	Tristate	139	143	169
PH[1]	PCR[113]	AF0 AF1 AF2 AF3	GPIO[113] E1UC[3] SOUT1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O O —	Tristate	25	145	173

Table 3-3 Functional port pin descriptions

PH[2]	PCR[114]	AF0 AF1 AF2 AF3	GPIO[114] E1UC[4] SCK_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	Tristate	58	146	175
PH[3]	PCR[115]	AF0 AF1 AF2 AF3	GPIO[115] E1UC[5] CS0_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	Tristate	28	147	177
PH[4]	PCR[116]	AF0 AF1 AF2 AF3	GPIO[116] E1UC[6] — —	SIUL eMIOS_1 — —	I/O I/O — —	Tristate	54	187	218
PH[5]	PCR[117]	AF0 AF1 AF2 AF3	GPIO[117] E1UC[7] — —	SIUL eMIOS_1 — —	I/O I/O — —	Tristate	51	190	221
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] — MA[2]	SIUL eMIOS_1 — ADC	I/O I/O — O	Tristate	21	191	222
PH[7]	PCR[119]	AF0 AF1 AF2 AF3	GPIO[119] E1UC[9] CS3_2 MA[1]	SIUL eMIOS_1 DSPI_2 ADC	I/O I/O O O	Tristate	—	192	223
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC	I/O I/O O O	Tristate	65	193	224
PH[9][7]	PCR[121]	AF0 AF1 AF2 AF3	GPIO[121] — TCK —	SIUL — JTAGC —	I/O — I —	Input, weak pull-up	128	174	205
PH[10][7]	PCR[122]	AF0 AF1 AF2 AF3	GPIO[122] — TMS —	SIUL — JTAGC —	I/O — I —	Input, weak pull-up	131	172	203

Table 3-3 Functional port pin descriptions

PJ[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] — SDA1 —	SIUL — I2C1 —	I/O — I/O —	Tristate	129	47	62
PJ[1]	PCR[129]	AF0 AF1 AF2 AF3	GPIO[129] — SCL1 —	SIUL — I2C1 —	I/O — I/O —	Tristate	122	43	58
PJ[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] CS1_1 — —	SIUL DSPI_1 — —	I/O I/O — —	Tristate	109	41	56
PJ[3]	PCR[131]	AF0 AF1 AF2 AF3	GPIO[131] CS2_1 — —	SIUL DSPI_1 — —	I/O O — —	Tristate	107	39	54
PJ[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] CS1_2 — —	SIUL DSPI_2 — —	I/O O — —	Tristate	—	37	52
PJ[5]	PCR[133]	AF0 AF1 AF2 AF3	GPIO[133] CS1_0 E0UC[6] —	SIUL DSPI_0 eMIOS_0 —	I/O O I/O —	Tristate	—	35	50
PJ[6]	PCR[134]	AF0 AF1 AF2 AF3	GPIO[134] CS2_0 E0UC[7] —	SIUL DSPI_0 eMIOS_0 —	I/O O I/O —	Tristate	—	29	44
PJ[7]	PCR[135]	AF0 AF1 AF2 AF3	GPIO[135] CS3_0 CS0_0 —	SIUL DSPI_0 DSPI_0 —	I/O O I/O —	Tristate	—	27	42
PJ[8]	PCR[136]	AF0 AF1 AF2 AF3	GPIO[136] CS4_0 SCK_0 —	SIUL DSPI_0 DSPI_0 —	I/O O I/O —	Tristate	35	154	185

Table 3-3 Functional port pin descriptions

PJ[9]	PCR[137]	AF0 AF1 AF2 AF3	GPIO[137] — SCK_1 —	SIUL — DSPI_1 —	I/O — I/O —	Tristate	106	152	183
PJ[10]	PCR[138]	AF0 AF1 AF2 AF3	GPIO[138] MA[2] — —	SIUL ADC — —	I/O O — —	Tristate	32	148	179
PJ[11]	PCR[139]	AF0 AF1 AF2 AF3	GPIO[139] — SOUT_1 —	SIUL — DSPI_1 —	I/O — O —	Tristate	113	82	101
PJ[12]	PCR[140]	AF0 AF1 AF2 AF3	GPIO[140] — SCK_2 —	SIUL — DSPI_2 —	I/O I/O I/O —	Tristate	—	81	100
PJ[13]	PCR[141]	AF0 AF1 AF2 AF3	GPIO[141] — CS3_1 —	SIUL — DSPI_1 —	I/O I/O O —	Tristate	114	78	98
PJ[14]	PCR[142]	AF0 AF1 AF2 AF3	GPIO[142] MA[1] CS4_1 —	SIUL ADC DSPI_1 —	I/O O O —	Tristate	105	77	97
PJ[15]	PCR[143]	AF0 AF1 AF2 AF3	GPIO[143] MA[0] — —	SIUL ADC — —	I/O O O —	Tristate	47	178	209
A[0]	—	—	—	CEBI	O	Output	—	—	233
A[1]	—	—	—	CEBI	O	Output	—	—	234

Table 3-3 Functional port pin descriptions

A[2]	—	—	—	CEBI	O	Output	—	—	235
A[3]	—	—	—	CEBI	O	Output	—	—	236
A[4]	—	—	—	CEBI	O	Output	—	—	237
A[5]	—	—	—	CEBI	O	Output	—	—	238
A[6]	—	—	—	CEBI	O	Output	—	—	240
A[7]	—	—	—	CEBI	O	OutputOutput	—	—	241
A[8]	—	—	—	CEBI	O	Output	—	—	242
A[9]	—	—	—	CEBI	O	Output	—	—	243
A[10]	—	—	—	CEBI	O	Output	—	—	247

Table 3-3 Functional port pin descriptions

A[11]	—	—	—	CEBI	O	Output	—	—	1
A[12]	—	—	—	CEBI	O	Output	—	—	4
A[13]	—	—	—	CEBI	O	Output	—	—	5
A[14]	—	—	—	CEBI	O	Output	—	—	7
A[15]	—	—	—	CEBI	O	Output	—	—	8
A[16]	—	—	—	CEBI	O	Output	—	—	9
A[17]	—	—	—	CEBI	O	Output	—	—	10
A[18]	—	—	—	CEBI	O	Output	—	—	12
A[19]	—	—	—	CEBI	O	Output	—	—	13

Table 3-3 Functional port pin descriptions

A[20]	—	—	—	CEBI	O	Output	—	—	14
A[21]	—	—	—	CEBI	O	Output	—	—	15
A[22]	—	—	—	CEBI	O	Output	—	—	—
A[23]	—	—	—	CEBI	O	Output	—	—	—
A[24]	—	—	—	CEBI	O	Output	—	—	—
A[25]	—	—	—	CEBI	O	Output	—	—	—
A[26]	—	—	—	CEBI	O	Output	—	—	—
A[27]	—	—	—	CEBI	O	Output	—	—	—
A[28]	—	—	—	CEBI	O	Output	—	—	—

Table 3-3 Functional port pin descriptions

CS[0]	—	—	—	CEBI	O	Output	—	—	252
CS[1]	—	—	—	CEBI	O	Output	—	—	23
D[0]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[1]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[2]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[3]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[4]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[5]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[6]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—

Table 3-3 Functional port pin descriptions

D[7]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[8]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[9]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[10]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[11]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[12]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[13]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[14]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—
D[15]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	—

Table 3-3 Functional port pin descriptions

D[16]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	248
D[17]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	249
D[18]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	250
D[19]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	251
D[20]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	253
D[21]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	254
D[22]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	255
D[23]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	256
D[24]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	19

Table 3-3 Functional port pin descriptions

D[25]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	20
D[26]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	21
D[27]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	22
D[28]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	24
D[29]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	25
D[30]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	26
D[31]	—	—	—	CEBI	I/O	Input, weak pull-up	—	—	28
EB[0]	—	—	—	CEBI	O	Output	—	—	18
EB[1]	—	—	—	CEBI	O	Output	—	—	239

Table 3-3 Functional port pin descriptions

EB[2]	—	—	—	CEBI	O	Output	—	—	—
EB[3]	—	—	—	CEBI	O	Output	—	—	—
OE	—	—	—	CEBI	O	Output	—	—	6
RW	—	—	—	CEBI	O	Output	—	—	11

[1]Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 -> AF0; PCR.PA = 01 -> AF1; PCR.PA = 10 -> AF2; PCR.PA = 11 -> AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

[2] Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

[3] 256 LQFP contains pads which may not be available in other packages.

[4] All WKUP pins also support external interrupt capability. The default state of all WKUP pins are pull-up state. See wakeup unit chapter for further details.

[5] NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.

[7] Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO. PC[0:1] are available as JTAG pins (TDI and TDO respectively). PH[9:10] are available as JTAG pins (TCK and TMS respectively). If the user configures these JTAG pins in GPIO mode the device is no longer compliant with IEEE 1149.1-2001.

Appendix A Preliminary Electrical Characteristic

A.1 General

This section provides electrical parametrics and electrical ratings for the CCFC2003PT microcontroller unit.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle; however, for production silicon these specification will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

A.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it. See **Table A-1**.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table. Connect unused inputs to the appropriate voltage level, either V_{SSH} and V_{DDH}. This device is not guaranteed to operate properly at the maximum ratings.

Table A-1 Absolute Maximum Ratings

Num	Rating	Symbol	Value	Unit
1	IO Supply Voltage	V_{DD5V}	-0.5 to +6.0	V
2	Core Supply Voltage	V_{DD}	-0.5 to +1.65	V
3	Input Voltage[1]	V_{IN}	-0.3 to +6.0	V
4	Injected input current on any pin during overload condition	I_D	-10 to 10	mA
5	Operating temperature range	T_{OPT}	-40 to +125	^{O}C
6	Storage temperature range	T_{STG}	-55 to +150	^{O}C

NOTES:

1. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

A.3 Electrostatic Discharge (ESD) Protection

Table A-2 ESD Protection Characteristics

Parameter[1,2]	Symbol	Value	Units
ESD target for human body model	HBM	2000	V
ESD target for charged device model	CDM	500	V
	CDM(corners)3	750	V

NOTES:

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temparature, unless specified otherwise in the device specification.
3. Corner pins are Pin 1,44,45,88,89,132,133,176 for LQFP176 package type.

   Corner pins are Pin 1,52,53,104,105,156,157,208 for LQFP208 package type

A.4 Fast internal RC oscillator (16 MHz) electrical characteristics

Table A-3 FIRC electrical characteristics

Symbol	Parameter	Condition	Vaule			Unit
			Min	Typ	Max	
V_{dd}	Input Supply Voltage		2.0		5.5	V
f_{FIRC}	Fast internal RC oscillator Output clock frequency			16		MHz
i_{FIRC}	Fast internal RC oscillator consumption			400		μA
t_{FIRC}	Fast internal RC oscillator start-up time			5		μs
$\Delta_{FIRCVAR}$	Fast internal RC oscillator variation in over temperature and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration.		-3		+3	%

A.5 Voltage Reference Electrical Characteristics

Table A-4 Vref electrical characteristics

Symbol	Parameter	Vaule			Unit
		Min	Typ	Max	
V_{dd}	Input Supply Voltage	2.0		5.5	V
Vref	Voltage reference output voltage		1.2		V
I_{ref}	Voltage reference consumption				

A.6 Power Management Electrical Characteristics

A.6.1 PMU Electrical Characteristics

Table A-5 PMU Electrical Characteristics

Symbol	Parameter	Vaule			Unit
		Min	Typ	Max	
3.3V LDO					
V_{dd}	Input Supply Voltage	3.6	5.0	6.0	V
V_{REG}	Regulator Output Voltage		3.3		V
I_{REG}	Regulator Output Current		80	100	mA
t_{REG}	Regulator Power up Time		100		μs
I_{CONS}	Regulator Current Consumption		8.5		μA
C_{REG}	Regulator External Ceramic capacitance	0.47	1	2.2	μF
R_{REG}	Regulator Equivalent Series Resistance (ESR)	5		300	mΩ
Low voltage detector					
V_{TH1P5V}	External 1.5V LDO LVD input supply voltage voltage threshold		1.5		V
$V_{HYS1P5V}$	External 1.5V LDO LVD V_{TH} hysterisis voltage		0.15		V
V_{TH3P3V}	3.3V LDO LVD input supply voltage voltage threshold		2.8		V

Table A-5 PMU Electrical Characteristics

$V_{HYS3P3V}$	3.3V LDO LVD V_{TH} hysterisis voltage		0.2		V
$V_{THavdd3P3V}$	5.0V supply voltage LVD input supply voltage voltage threshold		2.8		V
$V_{HYSavdd3P3V}$	5.0V supply voltage LVD V_{TH} hysterisis voltage		0.2		V
$V_{THavdd5P5V}$	5.0V supply voltage LVD input supply voltage voltage threshold		4.4		V
$V_{HYSavdd5P5V}$	5.0V supply voltage LVD V_{TH} hysterisis voltage		0.2		V
1.5V Power on reset					
V_{dd}	Input Supply Voltage	1.35	1.5	1.65	V
V_{TH}	Supply Voltage Trip Threshold		0.9		V
3.3V Power on reset					
V_{dd}	Input Supply Voltage	2.2	3.3	6.0	V
V_{TH}	Supply Voltage Trip Threshold		1.65		V
5.0V Power on reset					
V_{dd}	Input Supply Voltage	2.2	5.0	6.0	V
V_{TH}	Supply Voltage Trip Threshold		1.7		V

A.6.2 Power-Up Sequence

The 1.5 V VDD power supply must rise to 1.35 V before the VDD5V power supply rises above 2.8 V. This ensures that digital logic in the PLL or FIRC for the 1.5 V power supply does not begin to operate below the specified operation range lower limit of 1.35 V. The internal VDD5V POR will hold the device in reset as low as 2.8 V, VDD must be within specification before the VDD5V POR negate.

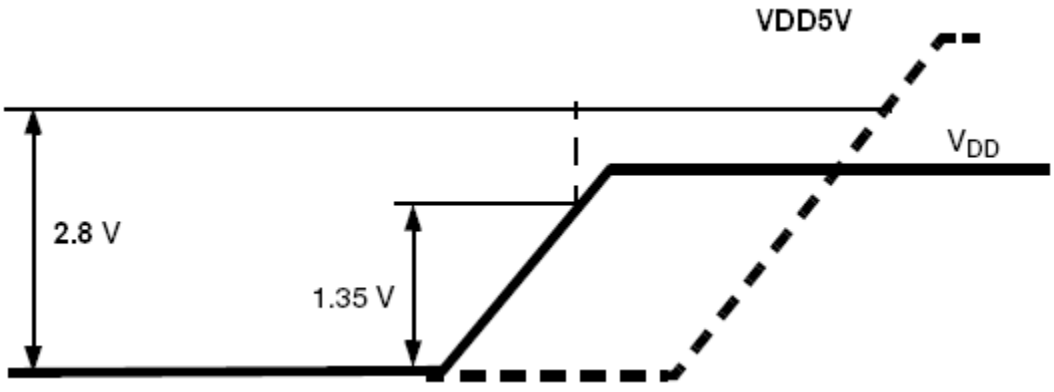


Figure A-1 Power-Up sequence

A.6.3 Power-Down Sequence

The only requirement for the power-down sequence with VDD5V grounded is if VDD decreases to less than its operating range(1.35V ~ 1.65V), VDD5V power must decrease to less than 2.8 V . This ensures that the digital 1.5 V logic, which is reset only by VDD5V POR and can cause the 1.5 V supply to decrease less than its specification value, resets correctly.

A.7 ADC Electrical Characteristics

Table A-6 ADC conversion characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{DDA}	Analog supply voltage	2.7	3.3/5.0	5.5	V
V_{REFH}	Reference supply voltage high			V_{DDA}	V
V_{REFL}	Reference supply voltage low		0		V
V_{AIN}	Conversion voltage range	0		V_{REFH}	V
T_A	Temperature range			125	℃
f_{ADC}	ADC clock frequency			16	MHz
f_{CONV}	12-bit conversion rate			1	MS/s
$I_{ADCVREFH}$	ADC VREFH consumption in running mode		550		uA
I_{ADCPWD}	ADC consumption in power down mode		1		uA
I_{ADCRUN}	ADC consumption in running mode		2		mA
t_{ADC_PU}	ADC power up delay		2		μs
t_s	Sampling time	3			clk
t_c	Conversion time		12		clk
C_S	ADC input sampling capacitance		6.4		pF
C_{P1}	ADC input pin capacitance		3		pF
DNL	Differential Nonlinearity (DNL)		±3		LSB
INL	Integral Nonlinearity (INL)		±8		LSB

Table A-7 ADC input leakage current

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	

Table A-7 ADC input leakage current

I_{LKG}	Input leakage current	T_A = - 125 °C	No current injection on adjacent pin	-2.5		2.5	uA

A.8 I/O pad electrical characteristics

A.8.1 I/O input DC characteristics

Table A-8 I/O input DC electrical characteristics

Symbol	Parameter	Conditions[1]		Value			Unit
				Min	Typ	Max	
V_{IH}	Input high level	V_{DD5V} = 5.0 V		0.65*VDD5V		VDD5V	V
V_{IL}	Input low level	V_{DD5V} = 5.0 V		VSS		0.35*VDD5V	
V_{HYS}	Input hysteresis	V_{DD5V} = 5.0 V			0.1*VDD5V		
I_{LKG}	Digital input leakage	No injection on adjacent	T_A = - 125 °C	-2.5		2.5	uA
I_{LOADD}	Digital IO input capitance	T_A = 25 °C				7	pF
I_{LOADC}	Analog/Digital IO input capitance	T_A = 25 °C				12	pF

NOTES:

1. T_A = - 40 to 125 °C, unless otherwise specified.

A.8.2 I/O output DC characteristics

Table A-9 I/O pull-up/pull-down DC electrical characteristics

Symbol	Parameter	Conditions[1]		Value			Unit
				Min	Typ	Max	
$\|I_{WPU}\|$	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD5V} = 5.0 V	pad_i_SPTP = 1	50		250	µA
$\|I_{WPD}\|$	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD5V} = 5.0 V	pad_i_SPTP = 1	50		250	µA

NOTES:

1. T_A = - 40 to 125 °C, unless otherwise specified.

Table A-10 Low Drive configuration output buffer electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
V_{OH}	Output high level low drive configuration	I_{OH} =5 mA, V_{DD5V} = 5.0 V, pad_i_SPTP = 1 (recommended)	0.8*VDD5V		VDD5V	V
V_{OL}	Output low level low drive configuration	I_{OL} = 5 mA, V_{DD5V} = 5.0 V, pad_i_SPTP = 1 (recommended)	0		0.1*VDD5V	V

NOTES:

1. T_A = - 40 to 125 °C, unless otherwise specified.

Table A-11 High Drive configuration output buffer electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
V_{OH}	Output high level High Drive configuration	I_{OH} = 10 mA, V_{DD5V} = 5.0 V, pad_i_SPTP = 1 (recommended)	0.8*VDD5V		VDD5V	V
V_{OL}	Output low level High Drive configuration	I_{OL} = 10mA, V_{DD5V} = 5V , pad_i_SPTP = 1 (recommended)	0		0.1*VDD5V	V

NOTES:

1. T_A = - 40 to 125 °C, unless otherwise specified.

A.8.3 PAD AC Specifications

Table A-12 Pad AC Specifications (V_{DD5V} = 5.0 V)[1]

Spec	SRC/DSC	Out Delay[2,4] L→H/H←L (ns)	Rise/Fall[3,4] (ns)	Load Drive(pF)
1	00	6.851/4.451	4.555/3.281	50
2		15.43/11.13	17.3/12.26	200

Table A-12 Pad AC Specifications (V_{DD5V} = 5.0 V)[1]

Spec	SRC/DSC	Out Delay[2,4] L→H/H←L (ns)	Rise/Fall[3,4] (ns)	Load Drive(pF)
3	01	8.792/6.219	8.797/6.153	50
4		27.06/19.59	34.85/24.39	200
5	10	16.14/11.57	7.265/6.387	50
6		25.51/19.47	19.49/14.45	200
7	11	14.28/10.39	9.375/7.228	50
8		32.15/23.8	35.16/24.86	200

NOTES:

1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.35 V to 1.65 V, V_{DD5V} = 5 V.
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. This parameter is guaranteed by characterization before qualification rather than 100% tested.
4. Delay and rise/fall are measured to 20% or 80% of the respective signal.

A.9 FMPLL Electrical Characteristics

A.9.1 FMPLL electrical characteristics

Table A-13 PLL electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
f_{PLLIN}	FMPLL reference clock[2]		8			MHz
f_{PLLOUT}	FMPLL output clock frequency		10M		500	MHz
f_{DUTY}	FMPLL output clock duty cycle		45	50	55	%
t_{LOCK}	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		200		µs
Δt_{LTJIT}	FMPLL period jitter,RMS	@500MHz,T_A = 25 °C		10		ps
I_{PD}	FMPLL power-down consumption				10	uA

NOTES:

1. V_{DD5V} = 5.0 V ± 10%, T_A = - 40 to 125 °C, unless otherwise specified.
2. PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode.

A.10 AC timing

A.10.1 IEEE 1149.1 interface timing

Table A-14 JTAG pin AC electrical characteristics[1]

#	Symbol	Characteristic	Min. Value	Max. Value	Unit
1	T_{CYC}	JTAG TCK period	100	—	ns
2	T_{PULSE}	JTAG TCK pulse width	40	60	ns
3	T_R	JTAG TCK rising time	—	5	ns
3	T_F	JTAG TCK falling time	—	5	ns
4	t_{TMSS}	JTAG TMS setup time	8	—	ns
4	t_{TDIS}	JTAG TDI hold time	6	—	ns
5	t_{TMSH}	JTAG TMS setup time	25	—	ns
5	t_{TDIH}	JTAG TDI hold time	25	—	ns
6	t_{TDOV}	JTAG TCK rising to TDO valid time	—	23	ns
7	t_{TDOI}	JTAG TCK falling to TDO invalid time	0	—	ns
8	t_{TDOHZ}	JTAG TCK falling to TDO tristate time	—	20	ns

1 JTAG timing specified at VDD = 1.35 V to 1.65 V, VDD5V = 4.5 V to 5.5 V.

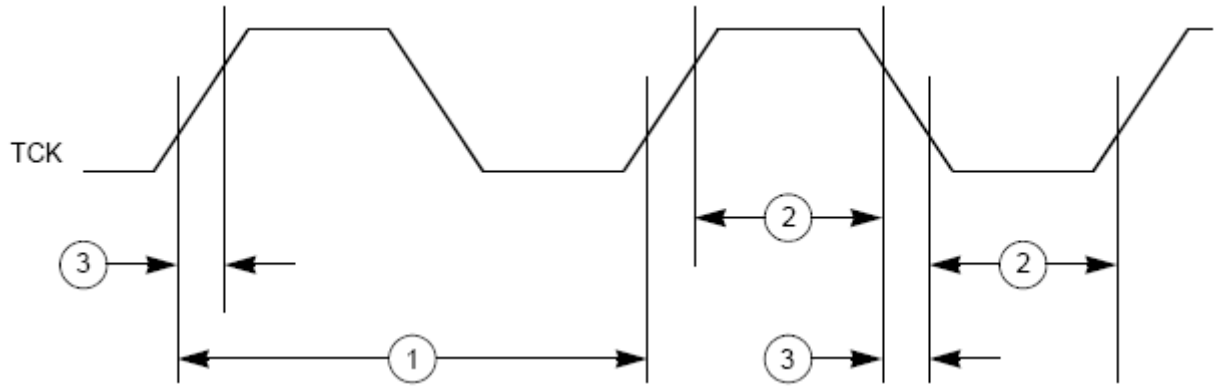


Figure A-2 JTAG test clock input timing

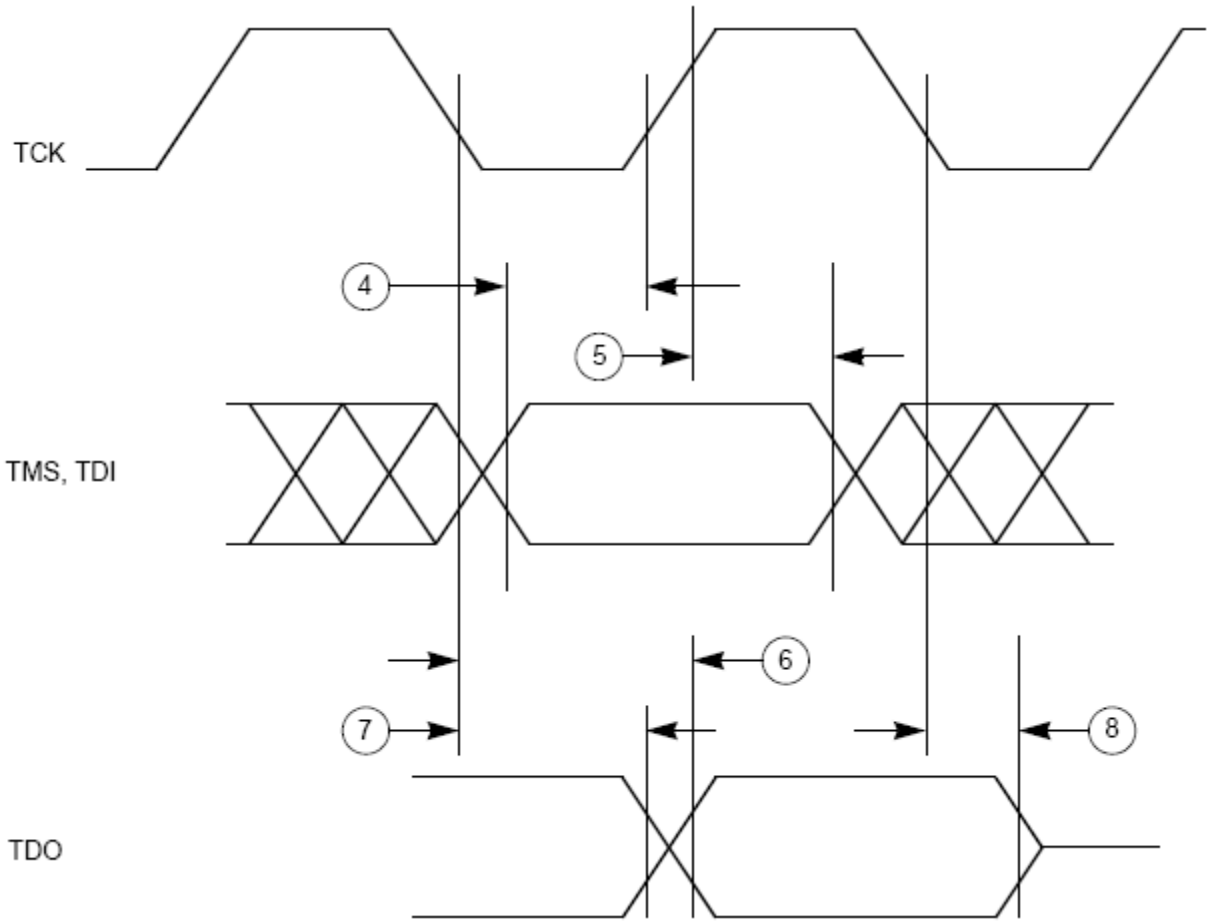


Figure A-3 JTAG test access port timing

A.10.2 DSPI AC timing

Table A-15 DSPI timing

#	Symbol	Characteristic	Min. Value	Max. Value	Unit
1	T_{CYC}	SPI SCK period	100	—	ns
2	T_{DELAY}	SPI PCS to SCK delay	35	—	ns
3	T_{DELAY}	SPI SCK to PCS delay	40	—	ns
4	T_{PULSE}	SPI SCK pulse width	50	—	ns
5	t_{DSET}	SPI data setup time	30	—	ns

6	t_{DHOLD}	SPI data hold time	-5	—	ns
7	t_{DELAY}	SPI data output time	—	10	ns
8	t_{DHOLD}	SPI data output hold time	-5	—	ns

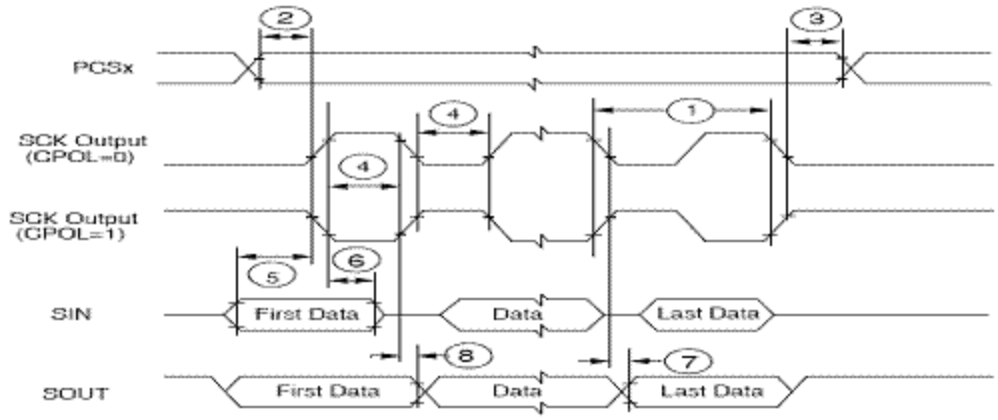


Figure A-4 DSPI classic SPI timing – master, CPHA = 0

A.10.3 eMIOS timing

Table A-16 eMIOS timing[1]

#	Symbol	Characteristic	Min. Value	Max. Value	Unit
1	T_{MIPW}	eMIOS input pulse width	4	—	t_{CYC}
2	T_{MOPW}	eMIOS output pulse width	1	—	t_{CYC}

1 eMIOS timing specified at VDD = 1.35 V to 1.65 V, VDD5V = 4.5 V to 5.5 V.

A.10.4 CLKOUT timing

Table A-17 CLKOUT timing[1]

#	Symbol	Characteristic	Min. Value	Max. Value	Unit
1	T_C	CLKOUT period	1	—	ns

2	T_{CDC}	CLKOUT duty cycle	45%	55%	T_C
3	T_{CRT}	CLKOUT rise time	—	3	ns
4	T_{CFT}	CLKOUT fall time	—	3	ns

1 eMIOS timing specified at VDD = 1.35 V to 1.65 V, VDD5V = 4.5 V to 5.5 V.

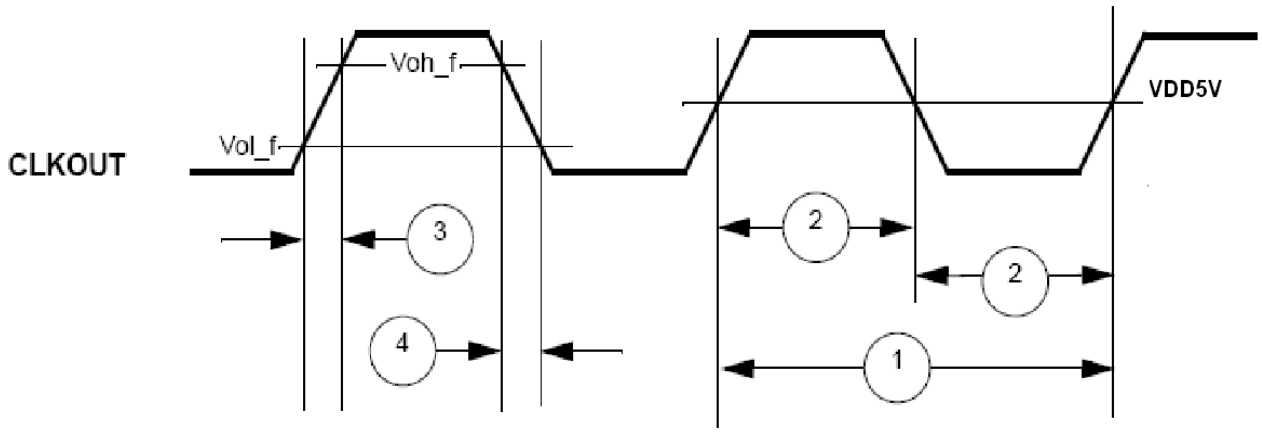


Figure A-5 CLKOUT timing

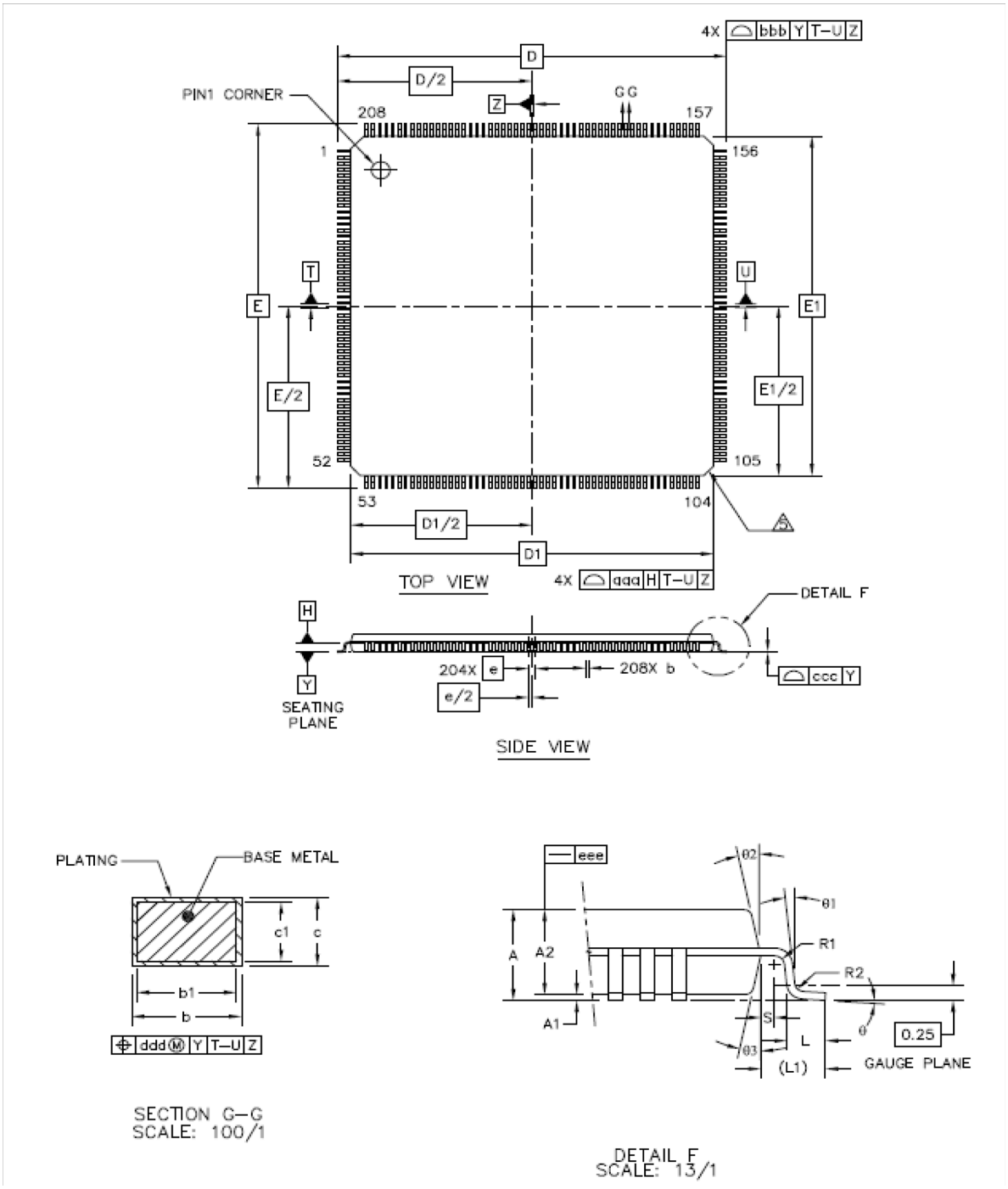
Appendix B Mechanical Specifications

B.1 General

CCFC2003PT is available in the following packages:

- LQFP208

B.2 LQFP208 Mechanical Drawing



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	30 BSC		
	Y	E	30 BSC		
BODY SIZE	X	D1	28 BSC		
	Y	E1	28 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		